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NRL Report 5227

# PROJECT VANGUARD REPORT NO. 36
## MINITRACK REPORT NO. 8, TIME STANDARD

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## PREFACE

As a part of its effort in the International Geophysical Year (July 1957 through December 1958), the United States is attempting to place a number of artificial satellites into earth-encircling orbits. Overall management of the joint Army-Navy-Air Force program is the responsibility of the Office of Naval Research, which established Project Vanguard at the Naval Research Laboratory to carry out the technical program.

The most basic problems created by an earth satellite in orbit are associated with proving that it is in fact orbiting, and with the measurement of its orbit. The Minitrack system was developed at the Naval Research Laboratory to provide acquisition and tracking of the satellite by radio techniques. A subminiature radio designed to operate continuously for a least two weeks is provided within the satellite to illuminate antennas at ground tracking stations. By phase-comparison techniques, these ground stations will measure the angular position of the satellite as it passes through the antenna beam, recording its "signature" automatically without the need for initial tracking information. Analysis of this signature will provide the complete angular history of the satellite passage in the form of direction cosines and time coordinates. These data will be quickly transmitted to a central computing facility for the computation and publication of ephemerides.

This report, one of a series describing the various parts of the Minitrack system, discusses the Minitrack system briefly and provides a detailed description of the time standard portion.

CONTENTS

## ABSTRACT

The "Minitrack" system for tracking an artificial earth satellite, which has been developed as a part of Project Vanguard, is described briefly, and the time standard equipment which provides the system time reference is described in detail. The measurements made by the Minitrack system are phase comparisons between signals received on five pairs of antennas. The time standard provides the means for synchronizing the system with WWV time signals to an accuracy of ±1 millisecond, the 500-cps separation frequency for the receivers, the means for synchronizing the operation of the digital phase meters with the standard time, and the time bases for the data records.

The detailed test specifications for the time standard, and details of the counters, are given in appendixes.


## PROBLEM STATUS

This is an interim report on one phase of the problem; work is continuing.

## AUTHORIZATION

NRL Problem A02-86
Project No. NR 579-000


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# PROJECT VANGUARD REPORT NO. 36

## MINITRACK REPORT NO. 8, TIME STANDARD

## INTRODUCTION

As a part of Project Vanguard, the "Minitrack" satellite tracking system has been developed to prove that the satellite is in an orbit and to determine the constants of the orbit. The general aspects of this system have been discussed in Ref. (1). Briefly, as shown in Fig. 1, it is a phase-comparison system using a low-power lightweight satellite-borne transmitter to illuminate an antenna field of the type shown in Fig. 2. Five phase comparisons are made to measure two of the direction cosines of a line connecting the center of the antenna system and the satellite. These measurements are made as a precise function of time as the satellite passes through the basic antenna pattern. The basic measurements are obtained from the north-south and east-west fine baselines. The medium and coarse baselines are used for ambiguity resolution only. A complete discussion of the rf system and the phase measurement system have been given in Refs. (2) and (3).

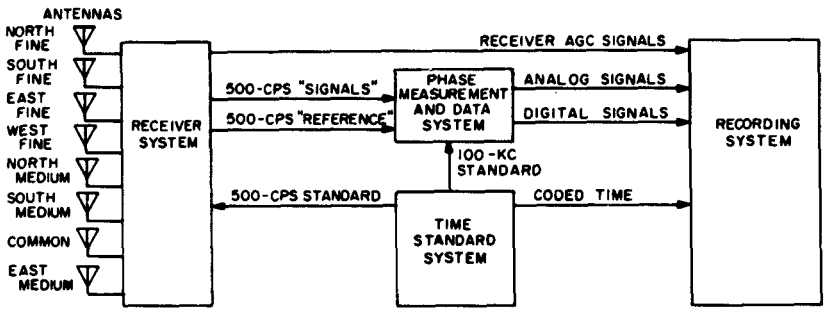


Fig. 1 - Minitrack ground station

The functions performed by the time standard as a part of the Minitrack system are:

1. To provide at each station a stable clock which will drift less than 1 millisecond per day, in order to permit all measurements of satellite passages to be made as precise functions of a standard time.

2. To provide means of synchronizing the output of this clock with a time reference, specifically the National Bureau of Standards time signals (Radio Station WWV).

3. To provide various frequencies derived from the basic 100-kc oscillator for other parts of the Minitrack system.

4. To provide all time signals needed by the various recorders, including a serial code readout of the standard time every 6 seconds.

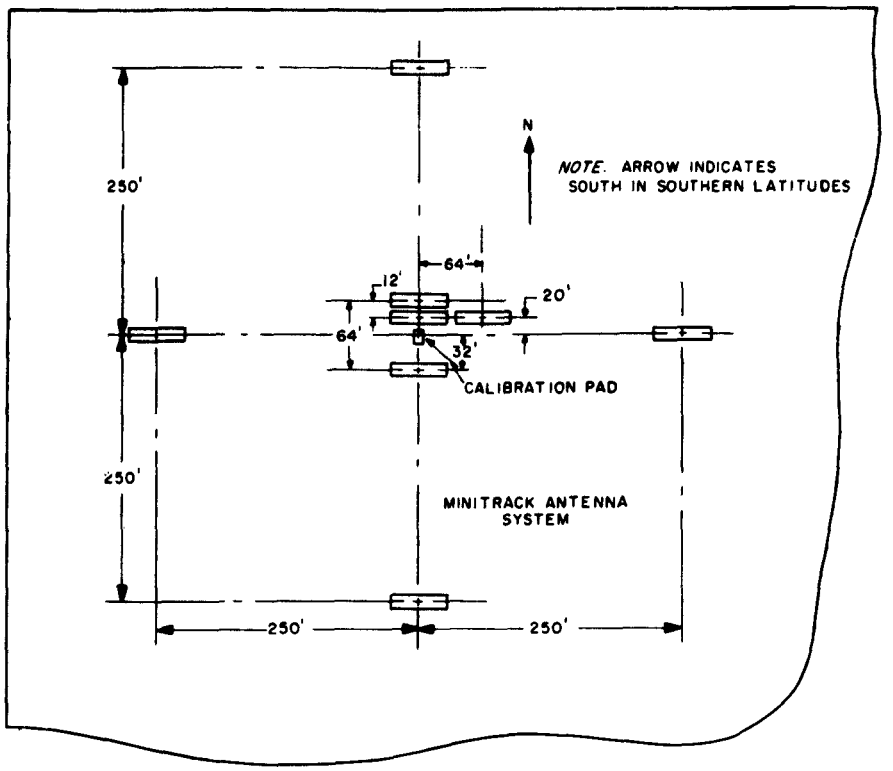


Fig. 2 - Antenna field layout

5. To provide a source of 500 cps, phase-coherent with and adjustable to the 1-cps output of the time standard, for separating the receiver frequencies (Ref. 2) and synchronizing "data-time," the trigger for the digital phase meters (Ref. 3) with the standard time.

The Minitrack satellite tracking network consists of a number of stations located in North America, West Indies, South America, Australia, and South Africa. In using the measurements made at various stations to determine the orbit of the satellite, a common time base is necessary. To provide some illustration of how closely the various time standards must be set, assume a 0.1-milliradian accuracy in the basic angle measurements. As the satellite passes over at an altitude of 300 miles with a velocity of 25,000 feet per second, it will have an angular rate of approximately 0.016 radians per second. At this angular rate a time error of 6.25 milliseconds will cause a 0.1-milliradian error in angle. At an altitude of 200 miles, this time error for a 0.1-milliradian angle error becomes slightly more than 4 milliseconds.

Tests conducted at the Naval Research Laboratory over a period of time indicate that a time standard can be adjusted to WWVH* with more than sufficient accuracy for this application. Uncertainties in propagation delay time and in the variations of propagation delay time are the major sources of error in adjusting the time standard. The tests

*The Bureau of Standards Time Station in Hawaii

indicate that the standards can be adjusted to ±1 millisecond, and the error introduced into the tracking data as a result of this time error will be negligible.

A block diagram of the time standard system is shown in Fig. 3; the phase measurement and recording systems are also shown to illustrate the relation of the two systems. The phase measurement system has been discussed in detail in Ref. 3. Each major block in the time standard will be discussed in a section of this report. Detailed test specifications are given in Appendix A.

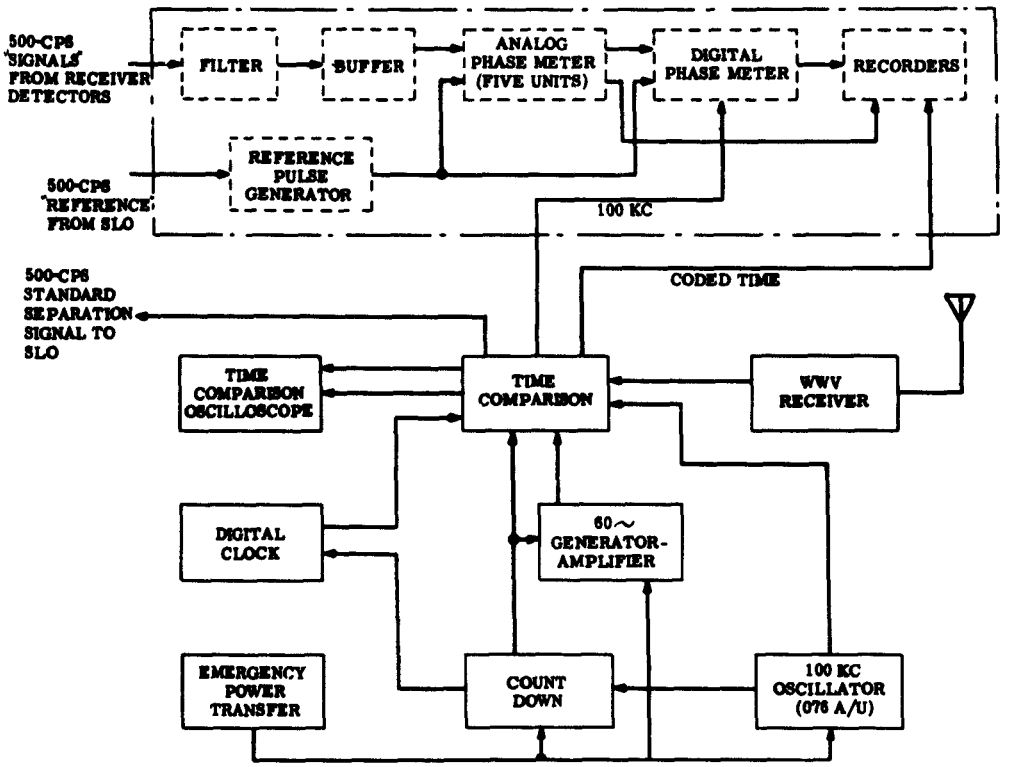


Fig. 3 - Time standard system

The basic unit in the time standard system is the 0-76A/U, 100-kc oscillator. The stable output of this oscillator is divided in the count-down unit to one cycle per minute (1 cpm) with various intermediate frequency outputs. The digital clock continues the division from the 1-cps output of the count-down unit to one pulse per 24 hours and presents the time as a neon lamp display and as a serial analog code, reading out every six seconds. The time-comparison chassis generates time-set and "standard time, data-time" coincidence pulses and also the 500-cps standard and 100-kc emergency standard frequencies; and converts the serial analog time code to a serial digital readout. The 60-cps generator-amplifier extracts the sixth harmonic of the 10-cps output of the count-down unit and amplifies it sufficiently to drive two "standard" clocks. The WWV receiver and a comparison oscilloscope are used in adjusting the output of the time standard to match the WWV signals. The emergency-power transfer contains the circuits to effect a switchover to a backup supply in the event of primary power failure.

## RF OSCILLATOR 0-76A/U

The basic frequency source used in the time standard is an 0-76A/U 100-kc rf oscillator (Western Electric D-175730-L2 frequency standard). The frequency-controlling crystal used in this oscillator is mounted in a double oven, with the outer oven controlled by a thermo-switch and the inner oven controlled by a temperature-sensitive bridge oscillator. The frequency-controlling crystal is driven in a bridge-type oscillator to generate a frequency of 100 kc. All associated circuits have been designed to minimize external causes of drift.

The 0-76A/U oscillator has a specified frequency stability of better than 1 part in $10^8$ per day. Tests after several months of operation indicate a stability of approximately 5 parts in $10^9$ per day with a predictable positive drift due to crystal aging. If the frequency were correctly adjusted at the start of a 24-hour period, a variation of 1 part in $10^8$ per day would give a time error of approximately 0.5 millisecond at the end of the 24-hour period.

Circuit details and operating considerations are completely explained in the instruction book for this equipment: "Instruction Book for R. F. Oscillator 0-76A/U," NAVSHIPS 91720.

## COUNT-DOWN UNIT

This unit is the basic frequency divider in the time standard. It receives the 100-kc output from the 0-76A/U oscillator, or from the "emergency" oscillator in the time-comparison chassis, and divides to 1 cpm with intermediate frequency outputs of 10 kc, 1 kc, 100 cps, 10 cps, and 1 cps. These outputs are available for use in the time standard and other parts of the Minitrack system. Provision is made, by means of a continuous phase-shifter, for adjusting the 1-cps output of the unit to coincide with the time reference (WWV). A block diagram of the unit is given in Fig. 4 and a schematic in Fig. 5.

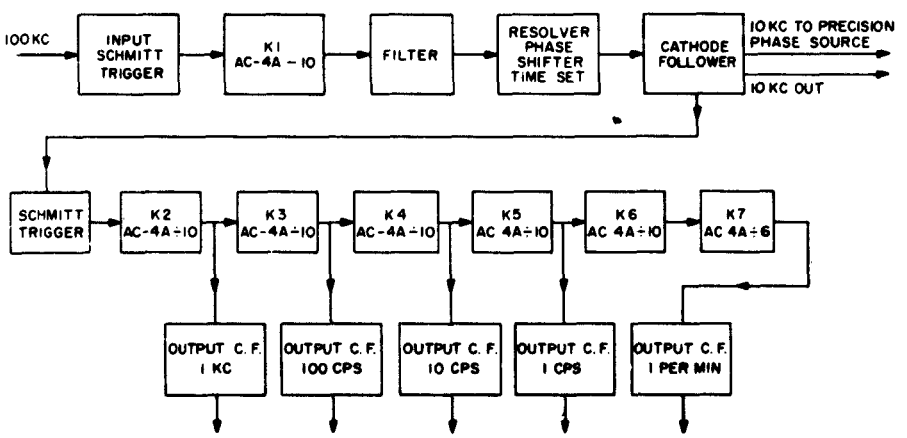


Fig. 4 - Count-down unit block diagram

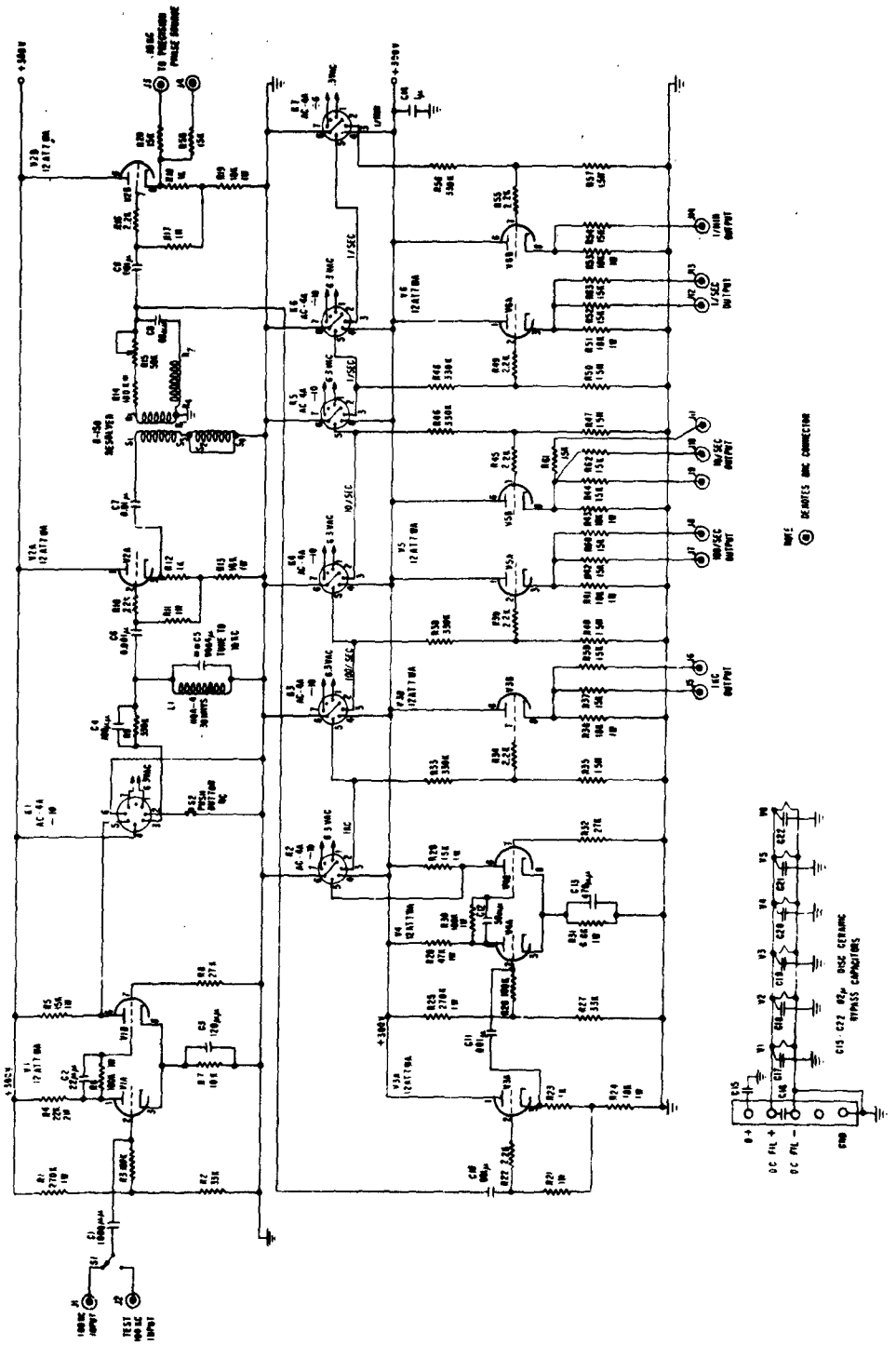

Fig. 5 - Count-down unit schematic

The input to the unit is normally the 100-kc, 20-volt peak-to-peak sine wave from the 0-76A/U oscillator; however, provision is made for switching to the "emergency" 100-kc oscillator in the time-comparison chassis in the event of failure of the 0-76A/U unit. The 100-kc sine wave is converted to a 100-kc square wave by the input Schmitt trigger, V1. This circuit is designed to exceed the fall rate (90 volts/microsecond) necessary to trigger the following counter (a Hewlett-Packard AC-4A decade counter) and will function properly with a rather large range of input amplitudes: approximately 10 volts to 130 volts peak-to-peak. A detailed discussion of the operation of the AC-4A counter is given in the Hewlett-Packard Instruction Book "Operating and Servicing Manual; Model AC-4A Decade Counter." The first AC-4A is used to divide the input 100 kc down to 10 kc. The 10-kc 6,4 wave* from the AC-4A is coupled to a tank, L1-C5, through C4-R9. The sine wave from the tank is coupled to one of the stator windings of a Reeves R-150 resolver through cathode follower V2A. The rotor, or output, windings are connected to R14, R15, and C8 to form a conventional continuous phase-shifter. The phase-shifter is used to adjust the 1-cps output of the count-down unit to match the one-per-second time-tick from N. B. S. radio station WWV.

The output of the phase-shifter is coupled to the precision phase generator through cathode follower V2B and to the second Schmitt trigger through cathode follower V3A. Four AC-4A decade counters follow the second Schmitt trigger, giving 6,4 wave outputs at 1 kc, 100 cps, 10 cps, and 1 cps. These in turn are followed by a standard AC-4A used for units-of-seconds display, and a modified AC-4A (divide by six) used for tens-of-seconds display. This modified counter also furnishes the 1-cpm output from the unit. The detailed changes necessary to convert a standard AC-4A to divide by 6 are given in Appendix B. Briefly, the changes consist of the removal of one bistable stage and the reconnection of the feedback loop from the third stage to the second to reverse its polarity of operation when adding in two counts at count four.

The various outputs are brought out through cathode followers as follows: 10 kc, V2B; 1 kc, V3B; 100 cps, V5A; 10 cps, V5B; 1 cps, V6A; 1 cpm, V6B. Protective series resistors are used in the outputs so that shorting of any of the outputs will not introduce an error in the basic time.

## DIGITAL CLOCK

The digital clock performs the following functions:

1. It continues the division of the basic oscillator frequency from the 1 cps of the count-down unit to one per 24 hours.
2. It provides a visual display of the time in hours, minutes, and tenths of minutes.
3. It provides a five-second serial-analog readout (repeated every six seconds or every minute) of the time in tens of hours, hours, tens of minutes, minutes, and tenths of minutes.

The block diagram (Fig. 6) shows the relationship of the various parts of the digital clock. These parts include the following:

1. A series of counters consisting of decade and modified decade units.
2. An electronic switch consisting of a sequence counter and gates.

*The output of the AC-4A decade counter, when triggered by uniformly-spaced negative pulses, is a rectangular wave which is low for six successive intervals between input pulses and then high for four successive such intervals. Such a wave is hereafter called a 6,4 wave.

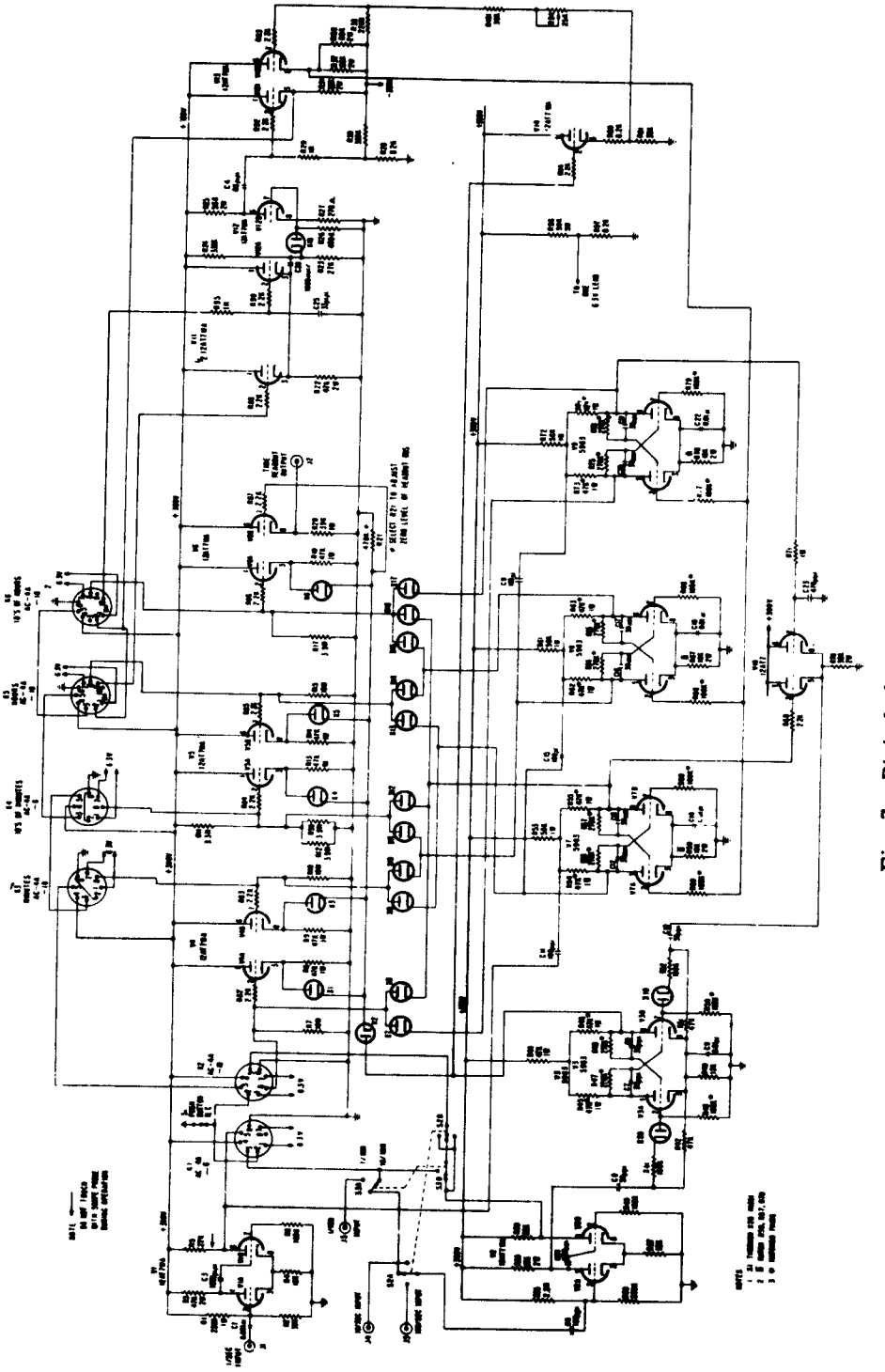

Fig. 7 - Digital clock schematic

This reset bus is otherwise held at zero volts by conduction through V13A, and its cathode-dropping resistors R31 and R59 which are returned to -200 volts. The coincidence pulse raises the voltage of the reset bus, thereby restoring K5 and K6 to "zero."

In normal operation (with readout every 6 seconds) the first decade counter, K1, must trigger K2 and also open the serial-readout gate. This would overload the output of K1, so a one-shot multivibrator, V2, is used after K1. The negative fall from the plate of V2B triggers K2, and the negative return of the plate of V2A, approximately 100 microseconds later, opens the serial-readout gate, V3 and X2, allowing the digital readout to start. The 100-microsecond delay assures that stable states have been reached in all counters before readout begins.

The level of the readout bus is set during six successive seconds by the staircase outputs of the decade counters K6, K5, K4, K3, and K2, and the "zero" staircase level. The five staircase outputs are fed to the readout bus through gates consisting of cathode followers V4, V5, and V6A and coupling diodes X1, X3, X4, X5, and X6.

The sequence counter, V7, V8, V9 and coincidence diodes X7 through X17 control the gates by holding the grids of the cathode followers below the base voltage of the staircases, raising one grid per second in sequence. As each grid is raised, the associated coupling diode connects the cathode to the readout bus until the grid is lowered 1 second later. The diode keeps the cathode follower disconnected from the bus for the other 5 seconds of the 6-second readout cycle.

Leads from the plates of V7B and V9B of the sequence counter go to the cathode-follower coincidence circuit, V10. The only time these plates are simultaneously low is on the count of 5. This negative fall, through diode X19, is used to close the serial-readout gate, V3, at which time V3B raises the level of the readout bus. During the sixth second of the readout cycle the gate holds the readout bus at the "zero" or maximum staircase level.

The same rise of V3B is applied to the grid of cathode follower V14. The output of V14 is applied to the grid of reset cathode follower V13B through R34. R34 is adjusted so that when the serial-readout gate is open the cathode of V13B, and therefore the reset bus of the sequence counter, is at ground potential. The positive pulse from V3B through V14 and V13B then raises the level of the bus (resetting the sequence counter to "zero") and holds it there until the next negative return of the plate of V2A reopens the readout gate.

The output from the readout bus through cathode follower V6B is used in the time-comparison chassis to determine the number of 10-per-second time-code pulses which are passed each second. In order to obtain an extra pulse at the beginning of each read-out, the "zero" level of the staircase output of the tens-of-hours counter, K6, is set to correspond with the "one" level from the other counters.

As is stated in the instruction book for the unit, the AC-4A counter has a "staircase" output of ten levels for its ten states ("zero" through "nine"). The divide-by-six counters have the "zero" through "five" levels. If the digital clock readout circuit in the time-comparison chassis is adjusted to give out one pulse for a "zero" level of the readout bus and ten pulses for a "nine" level, then the time-readout code will be as follows (the first pulse coming at the start of the time interval):

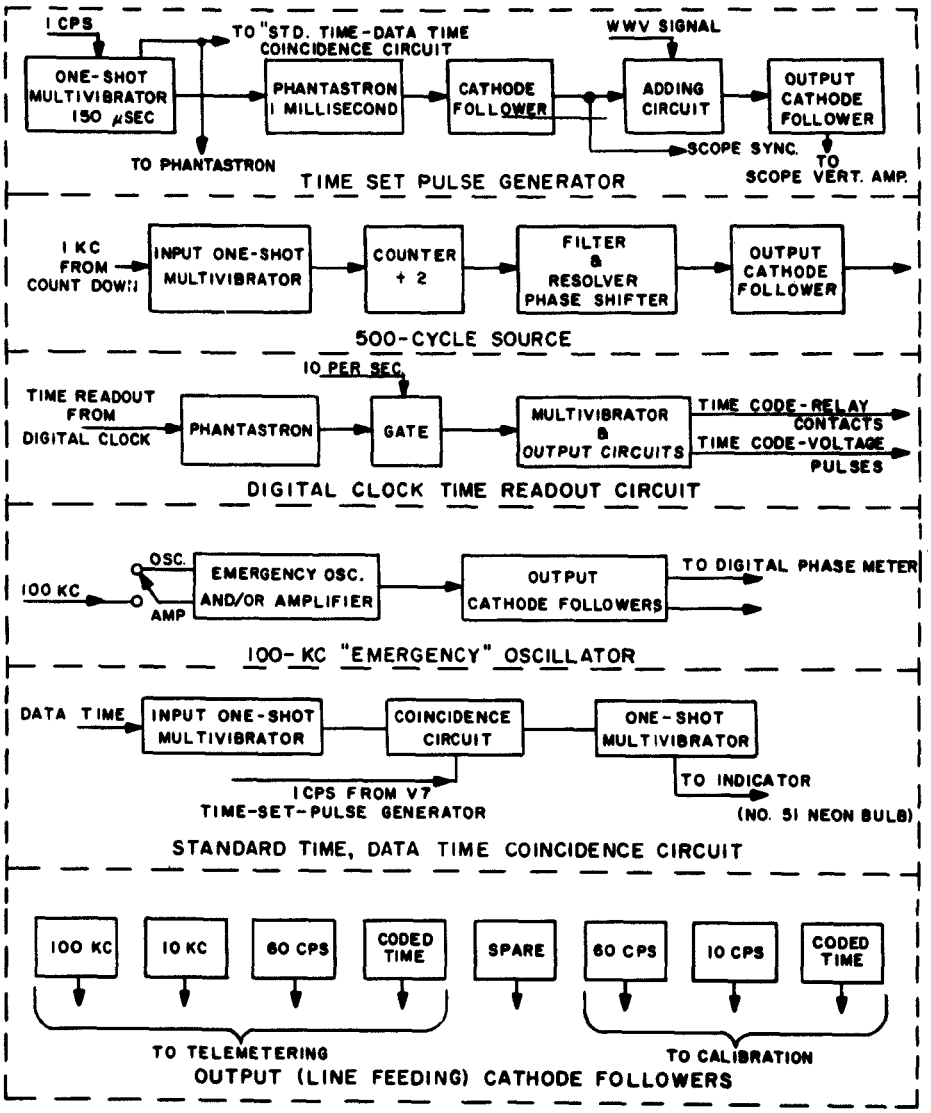


Fig. 8 - Block diagrams of time comparison chassis circuits

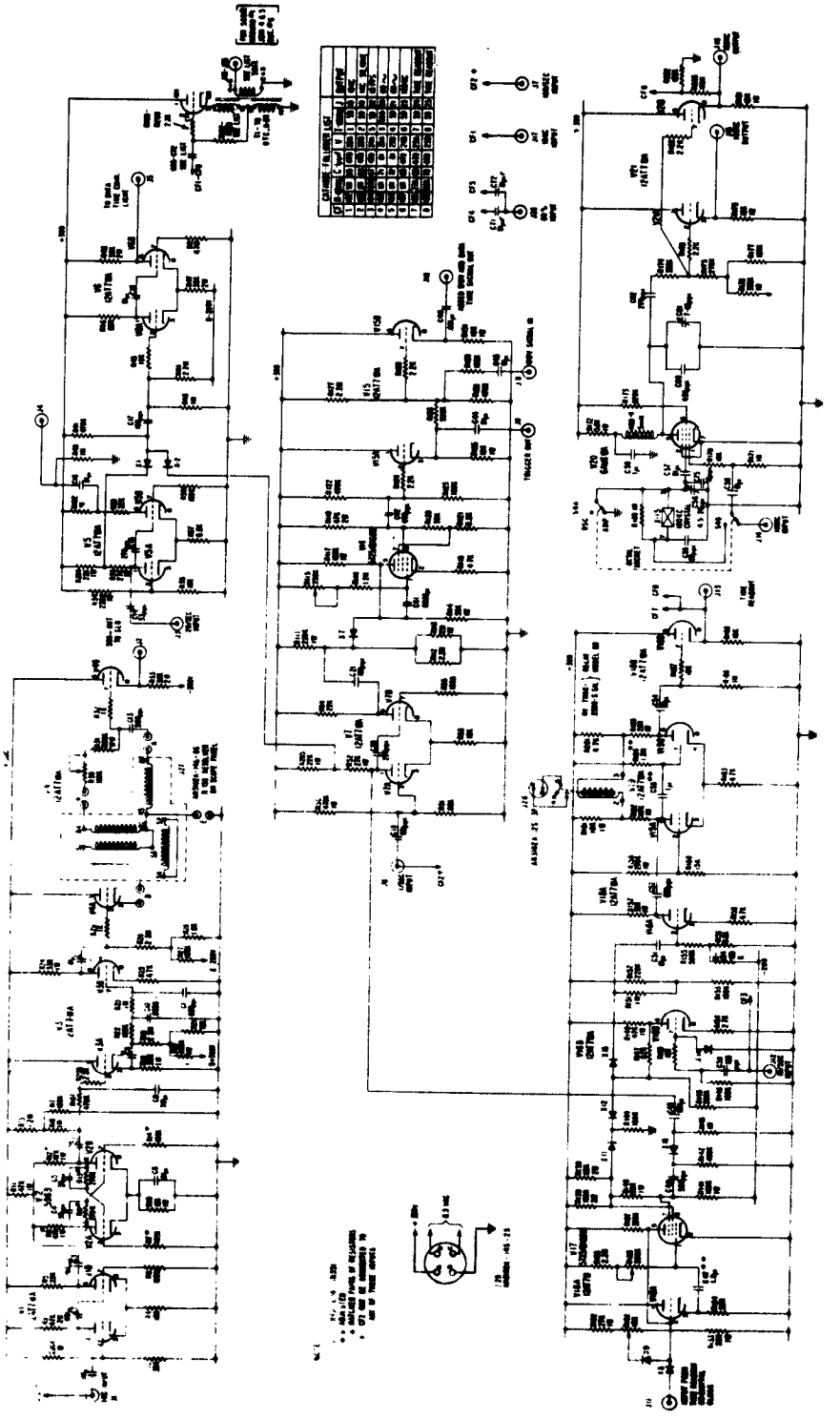

Fig. 9 - Time comparison chassis schematic

### Time-Set Pulse Generator

This circuit provides a synchronization pulse at the time of the negative fall of the 1-cps output from the count-down unit, a first marker at this time, and a second marker a millisecond later. The marker pulses and the WWV signal are added in a resistive network and are brought out for connection to the vertical amplifier of an oscilloscope. The pulses are generated by phantastron V14 (1 millisecond delay), which is triggered by the 1-cps output of the count-down unit through one-shot multivibrator V7 ("on" time, 50 $\mu$sec).

The positive rise of the phantastron screen is differentiated by C42 and R123 and coupled to output jack J8 through cathode follower V15A. Since the grid of V15A is returned to ground, the tube cuts off for a large negative signal on the grid and gives a cathode output of approximately 5 volts. This negative pulse, occurring at the phantastron return, and the positive pulse at the start of the rundown are added to the WWV signal in resistive network R126, R128, and R130, and this combined signal is coupled to output jack J10 through cathode follower V15B. The time comparison is made by connecting J8 to the synchronization input of the time-comparison oscilloscope and J10 to the vertical amplifier, and adjusting the time-set phase-shifter in the count-down unit until the markers are properly aligned with the WWV time-tick (with the negative marker at the end of the first cycle of the WWV time tick).

### 500-cps Source

The 500-cps source provides a 500-cps separation-signal (to the special local oscillator unit in the receiver rack) which is locked to the 0-76A/U basic clock oscillator. In addition, it incorporates a phase shifter which is used to set the data time (counted-down 500-cps "reference" from the special local oscillator) in coincidence with the standard-time output. The input to the 500-cps source is the 1-kc 6,4 wave from the count-down unit.

The input signal is shaped by the input multivibrator V1. This multivibrator in turn triggers a binary counter, V2. The 500-cps square wave from the binary counter is passed through low-pass filter R191-C8, cathode follower V3A, the two low-pass filters R22-C10 and R23-C11, and amplifier V3B. The sine wave out of V3B is coupled to the resolver through cathode follower V4A. The two stator windings of the Reeves R-150 resolver are connected to R30, R31, and C13 to form a conventional resolver phase shifter. V4B is the output cathode follower for the 500-cps source. The output signal is a 40-volt peak-to-peak sine wave.

### Digital-Clock-Readout Circuit

The digital-clock-readout circuit converts the serial-analog time readout of the digital clock into a modified serial-digital code and presents this output both as relay closures and as voltage pulses from a low-impedance source. The basic circuit consists of a phantastron with its run-down time controlled by a variation in the lower plate-clamping level proportional to the output level from the digital clock. This phantastron in turn controls a gate which allows the 10-cps output of the count-down unit to trigger a one-shot multivibrator, giving a relay-closure or a voltage-pulse output. The phantastron is adjusted by means of R190 and R136 so that 1 cps is obtained for the "zero" level out of the digital clock and 10 cps for the "nine" level. As was stated in the discussion of the digital clock, the "zero" level of the tens-of-hours counter is adjusted to be the same as the "one" level in the other counters. This means that the start of a readout is marked by one extra pulse.

The serial-analog code from the digital clock is coupled to the phantastron plate, V17, by diode X8. Diode X9 is a clamp on the upper level of the plate. Diodes X11, X12, and X13, in conjunction with plate divider R147,R145 and bias divider R152,R153, form a gate. This gate allows the 10-cps output of the count-down unit to trigger the timing-output multivibrator during the time the phantastron is running down. During the run-down time the screen voltage is high, X11 is conducting, and X12 is cut off. The dc levels of divider R147,R145 and R152,R153 are such that the pulses from amplifier V16B pass through diode X13 under these conditions. When the screen of the phantastron is down (gate closed), X11 is cut off and R144 is, in effect, in parallel with R145. This lowers the dc level of the divider to the point where the pulses out of amplifier V16B will not pass through diode X13. The gate output is amplified and inverted in V18A (biased beyond cutoff to discriminate against any spurious pulses) and triggers the timing one-shot multivibrator V19. The multivibrator has a relay between plates to give time code in the form of contact closures. Voltage output pulses are brought out through the output cathode follower V18B, and are also connected to two of the line-feeding cathode followers (CF7 and CF8).

### 100-kc "Emergency" Oscillator

A 100-kc crystal-controlled oscillator is included in the system as a backup for the 0-76A/U. It has sufficient stability after warm-up to be used as a timing oscillator for short periods (up to 2 hours). The oscillator, V20, is a conventional electron-coupled oscillator; C61 tunes the plate tank, and C56 adjusts the frequency over a very limited range. When the 0-76A/U is in use, the emergency oscillator is used as an amplifier for the 100 kc (switch S4). The 100 kc is brought out through cathode followers V21A and V21B and through line-feeding cathode follower CF6.

### "Standard Time, Data Time" Coincidence Circuit

The function of the "standard time, data time" coincidence circuit is to give a visual indication (by a neon bulb on the phase-measurement console) of coincidence of the two times.

Data time, the counted down "reference" from the special local oscillator, is shaped by a one-shot multivibrator, V5. A tap on the first plate is directly coupled to the cathode of diode X1. The 1-cps output of the count-down unit, shaped by the one-shot multivibrator in the time-set-pulse circuit, is coupled to the cathode of diode X2. A positive pulse on one cathode will not change the diode plate level significantly, but positive pulses on both cathodes will allow the plates to rise toward the level determined by divider R41,R43. (The actual swing is determined by the one-shot multivibrator with the lowest plate level in the triggered condition.) This positive rise triggers the output one-shot multivibrator V6, which was designed to operate between +300 and -200 volts dc so that the plate potential of the normally-on tube is low with respect to ground (standby state) and the indicating neon bulb and series resistor can be connected directly from plate to ground. The bias on V6A is sufficient that partial coincidences will not trigger the multivibrator.

### Output Cathode Followers

Eight output cathode followers are included for coupling the various outputs to a 500-ohm or 50-ohm line. A transformer (U.T.C. type A24) is used in the cathode of the cathode followers to couple to the lines. In the case of the lower frequency signals and the time readout pulse, only the leading and falling edges of the 6,4 waves or pulses are coupled into the line (a short time constant is used in the grid circuit). The turns ratio used depends upon the impedance of the line and the driving voltage available at the grid.

## 60-CPS GENERATOR-AMPLIFIER

A stable source of 60 cps is needed to perform various functions in the Minitrack system – for example, to provide a reference frequency for the telemetering recorders. It was also found desirable to have sufficient power available to drive two "standard" electric panel clocks. A block diagram of the amplifier is given in Fig. 10 and a schematic in Fig. 11.

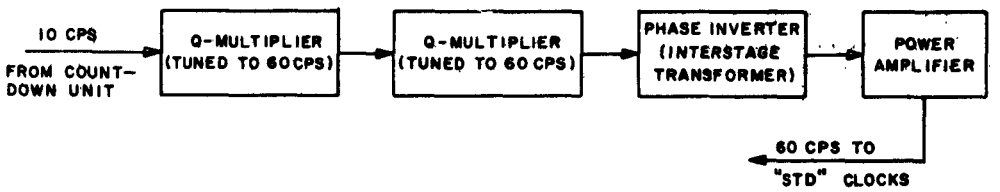


Fig. 10 - 60-cps generator-amplifier block diagram

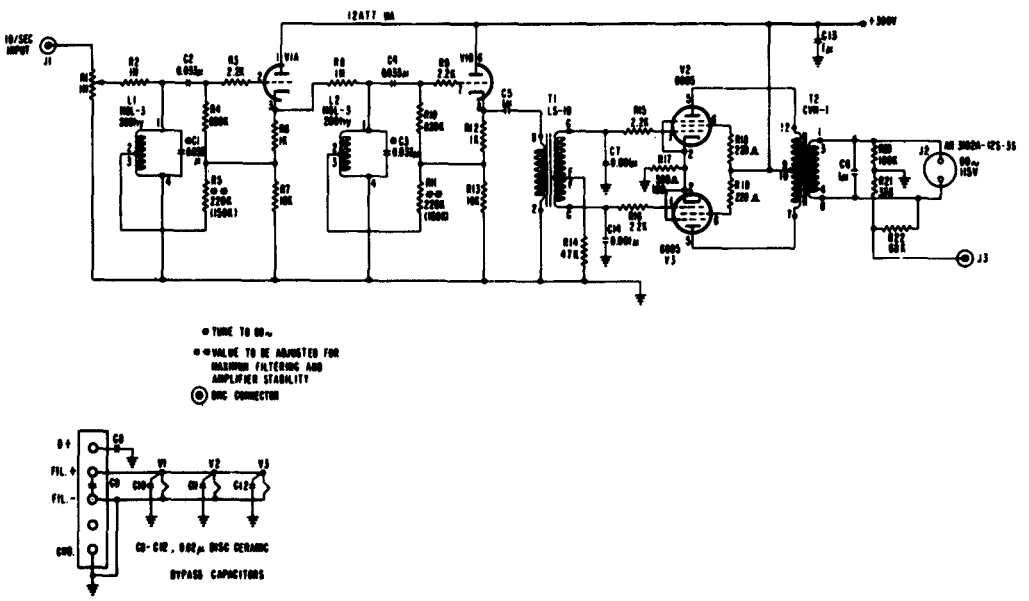

Fig. 11 - 60-cps generator-amplifier schematic

The sixth harmonic of the 10-cps 6,4 wave from the count-down chassis is extracted by the two Q-multiplier stages, V1A and V1B. Both tanks are tuned to 60 cps, and sufficient positive feedback is applied to give an effective Q of over 100. The circuit values shown in the schematic provide a margin of approximately two as far as stability is concerned. The signal from the second Q-multiplier stage, V1B, is coupled through an

interstage transformer to a class-A push-pull amplifier. The load, one or two "standard" electric clocks, is connected to the secondary of the output transformer. In addition, provision is made for connecting the output of the amplifier to the time-comparison chassis and through its line-driving cathode followers to the various other parts of the system.

## EMERGENCY-POWER TRANSFER

At some of the more distant stations, it may not be possible to receive standard-time signals at all times. A loss of 60-cps power at the station for even a short time could mean the loss of a time reference until reception of a time signal. In order to cover this possibility, the basic units in the time standard (the 0-76A/U oscillator, the count-down unit, the 60-cps amplifier, and the emergency-power transfer) are operated from a dc filament supply with floating battery, and obtain their B+ through the emergency-power transfer. If the B+ from the normal power source drops 8 volts, the emergency-power chassis transfers the load to a backup battery.

The 0-76A/U oscillator requires a regulated 135 volts dc at approximately 40 milliamperes. All other units require 300 volts dc. It was decided to incorporate a regulator in the emergency-power transfer to supply the oscillator power from the 300-volt supply. A block diagram of the emergency-power transfer is shown in Fig. 12, and a schematic in Fig. 13.

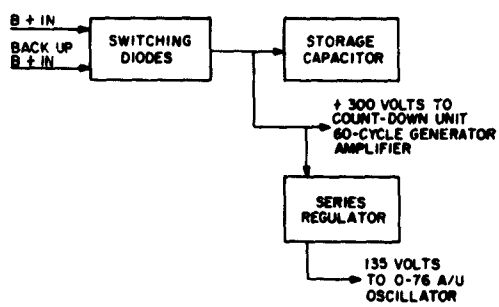


Fig. 12 - Emergency-power transfer block diagram

The 135-volt regulator is a series-tube type. V4 is a reference tube, V3 the amplifier, V2 the series regulator, and V5 a limiter for the grid of V2 (this limits the dc output voltage to +150 volts). This output voltage is adjusted to 135 volts dc by R13. M1 monitors the regulator output.

The normal B+ supply and the backup battery are connected to diodes X1 and X2 so that the power source with the higher voltage will supply the current to the load. The backup battery supplies the total current when the normal power supply drops 8 volts. Diode X2 is shunted by R15 to provide a charging current for the 300-volt nickel-cadmium backup battery. The "charge-operate" switch makes provision for the initial charging of C3 from the normal B+.

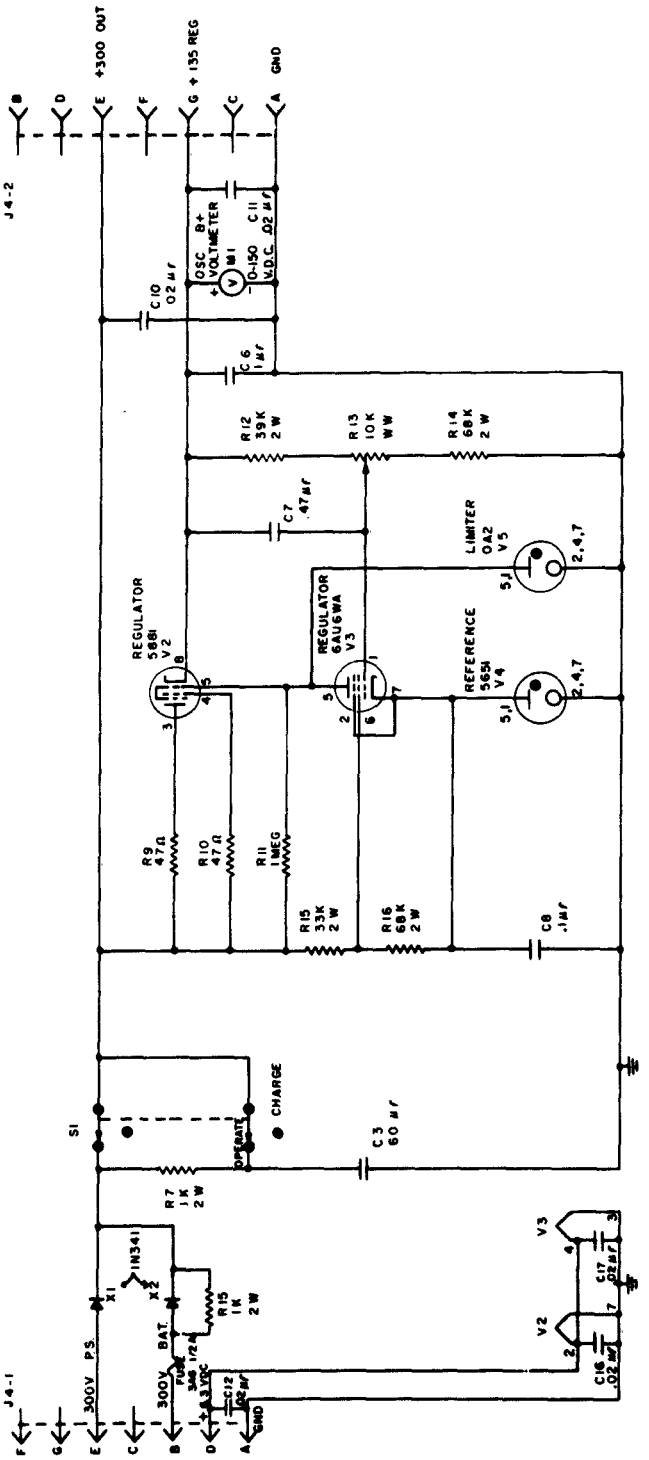


Fig. 13 - Emergency-power transfer schematic

## PRECISION PHASE GENERATOR

The precision phase generator is not an operational part of the time standard. It is a test signal source used in checkout and calibration of the phase meters (*Ref.* 3) and for certain system tests. It is included in the time standard rack because room and power are available, and because this location provides easy interconnection between the count-down unit and the precision phase generator.

The precision phase generator furnishes a 500-cps sine wave whose phase, with respect to the 500-cps standard, can be varied in a known and continuous manner. If it is to be used as an absolute phase source, a zero measurement must be made. Provision is made for phase-modulating the output of the precision phase generator up to $\pm 10^{\circ}$ from 0 to approximately 40 cps. A block diagram of the unit is given in Fig. 14 and a schematic in Fig. 15.

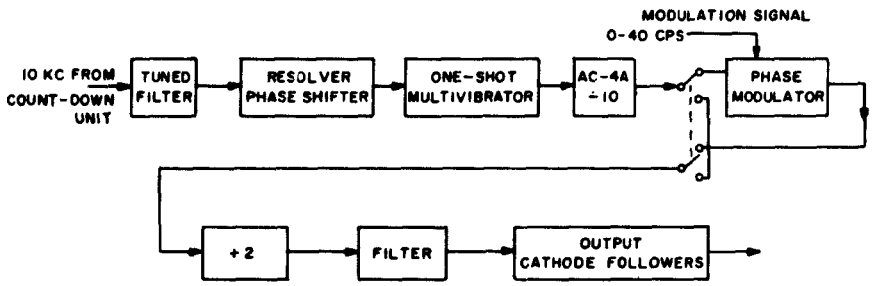


Fig. 14 - Precision phase generator block diagram

The 10-kc sine wave from the count-down unit is connected to the input of the unit. Capacitor C2, in conjunction with a 15K series resistor in the count-down unit, acts as a low-pass filter. This signal is coupled through cathode follower V1A to a phase inverter, V1B, whose outputs are coupled to cathode followers V2A and V2B. A $90^{\circ}$ phase-shift network is connected between the cathodes of these stages. Two signals $90^{\circ}$ out of phase are now available for feeding the two stator windings of a resolver used as a continuous phase shifter. This type of phase shifter was found to be slightly more accurate than the type used in the count-down unit; however, it requires careful adjustment of the $90^{\circ}$ phase shift (R15), and the amplitude of the two signals must be equal (R12). The signals are coupled to the stator windings of the resolver through cathode followers V3A and V3B. The output of the resolver phase-shifter is coupled through cathode follower V4A to Schmitt trigger circuit V5 which is designed to trigger the Hewlett-Parkard AC-4A decade counter (see the discussion of the count-down unit). The output of the AC-4A is a 1-kc 6,4 wave. A phase modulator can be switched in at this point if desired. The 1 kc is counted down to 500 cps by the binary counter V6. The 500-cps square wave is passed through three low-pass filters, amplified in V7B, passed through two additional low-pass-filter sections, and appears at the grid of cathode follower V8 as a sine wave of approximately 20-volt peak-to-peak amplitude. A low-value potentiometer is used in the cathode of V8 so that the output level can be adjusted without introduction of phase shift. V9A is the output cathode follower.

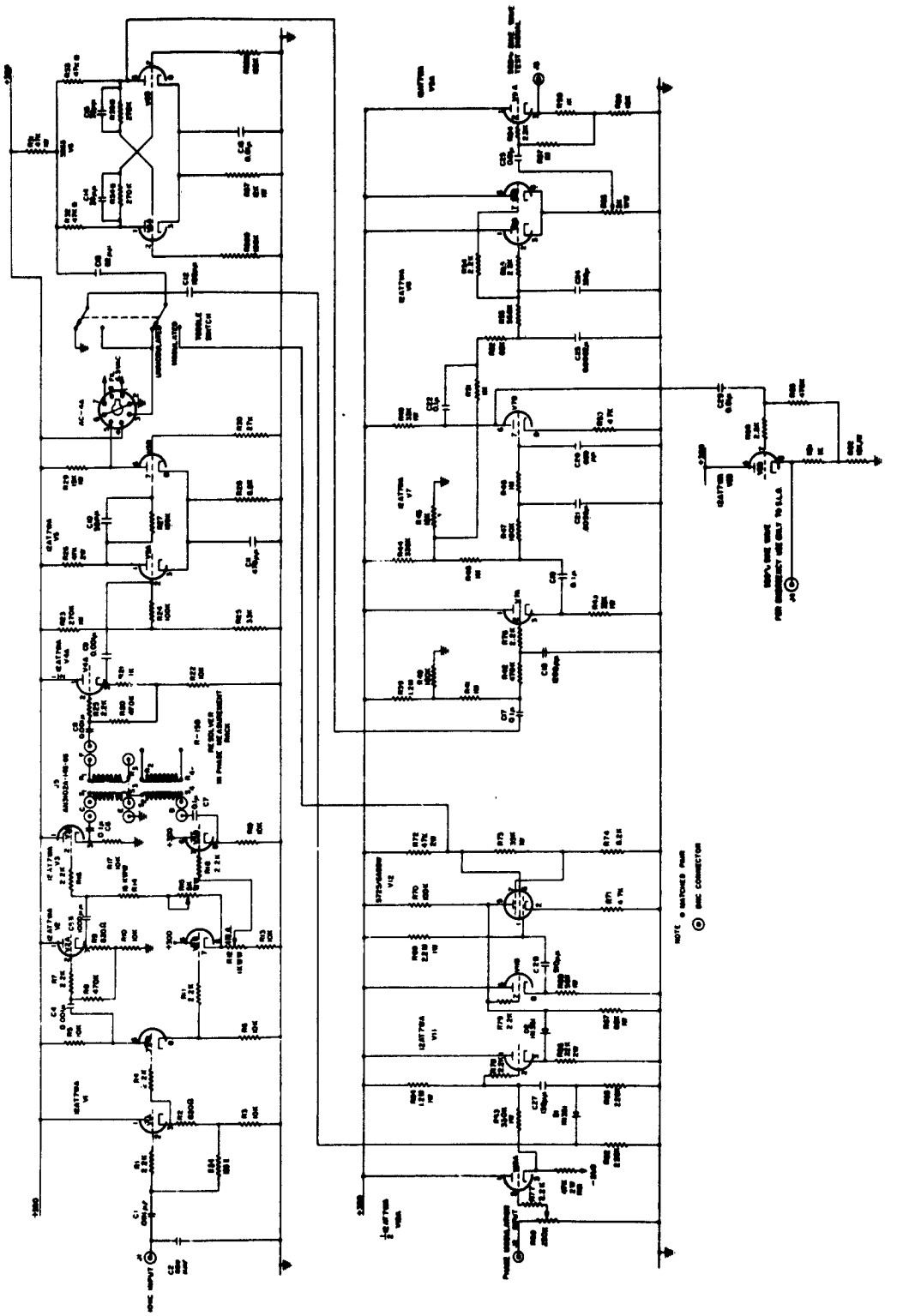

Fig. 15 - Precision phase generator schematic

The resolver used with the precision phase generator is mounted on the console of the phase measurement rack. It is geared to a counter which indicates degrees and tenths of a degree phase change. The measured run-out error of the resolver phase-shifter is less than $2^{\circ}$ throughout $360^{\circ}$. This error occurs at 10 kc and is reduced directly as the frequency division; at 500 cps this error is less than $0.1^{\circ}$ of phase.

The cathode follower V9B furnishes a 500-cps output which can be used to feed the special local oscillator unit in case of failure in the time comparison chassis.

It was stated in a previous paragraph that a phase-modulator could be switched in at the 1-kc point if so desired. This modulator is made up of a phantastron, V12 and V11B, and two cathode followers, V10A and V11A. If the modulator is switched in, and no signal is connected to the modulator input, a fixed phase-shift of approximately $25^{\circ}$ will occur because of the run-down time of the phantastron as determined by the standby upper and lower clamping levels. A signal connected to the modulation input is directly coupled to and controls the upper clamping level of the phantastron, thereby producing a variable delay or phase-modulation proportional to this signal.

## WWV RECEIVER

A commercial WWV receiver (Berkeley, Model 5590) is included in the time standard rack for reception of the WWV signal. The receiver is a crystal-controlled double-conversion superheterodyne with provision for switching to the various standard WWV frequencies. The sensitivity and selectivity of this receiver are essentially the same as that of the better communications receivers. The instruction book for this equipment gives detailed information.

## OPERATION

The arrangement of the various units (electronic chassis and power supplies in the rack and the rack control panel) is shown in Fig. 16. The intra-rack power wiring is shown in Fig. 17 and the intra-rack signal connections in Fig. 18.

Provision is made on the control panel for all switching necessary in the operation of the time standard, for monitoring primary power, and for indicating the total hours of equipment operation. The dc filament supply for the chassis listed in the discussion of the emergency-power transfer is built into the rack, and its controls are mounted on the control panel. The total drain from the primary power source by the time standard rack is approximately 1550 volt-amperes at 120 volts ac.

The various outputs from the time standard are brought out on two signal ports. One port contains the various signals concerned with the basic Minitrack system and the other the timing signals used for auxiliary functions.

A 3-inch oscilloscope (Tektronix Type 310) is mounted in the rack for use in adjusting the time standard to WWV. Except for the 6-volt filament battery and the "emergency" B+ battery, all components of the time standard are contained in the 24 x 22 x 77-inch rack shown in Fig. 16.

The following brief paragraph on each unit in the time standard will describe the adjustments and measurements necessary to put the equipment in operation. No attempt will be made to cover operational procedures, troubleshooting, or preventive maintenance in this report; however, detailed test specifications are given in Appendix A.

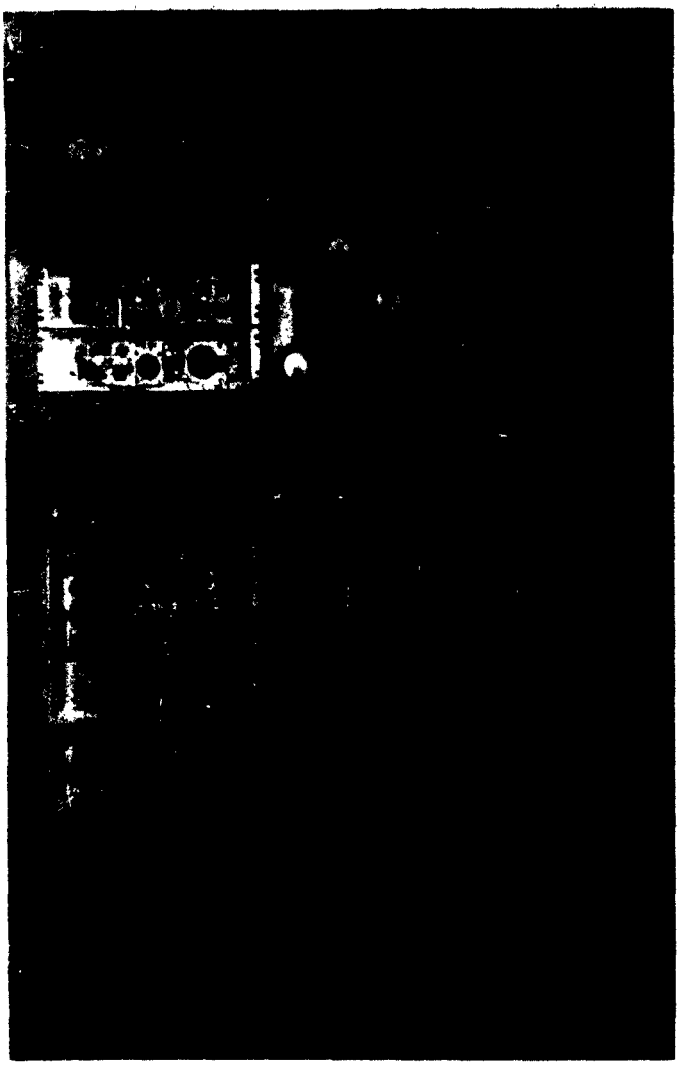

Fig. 16 - The time standard equipment

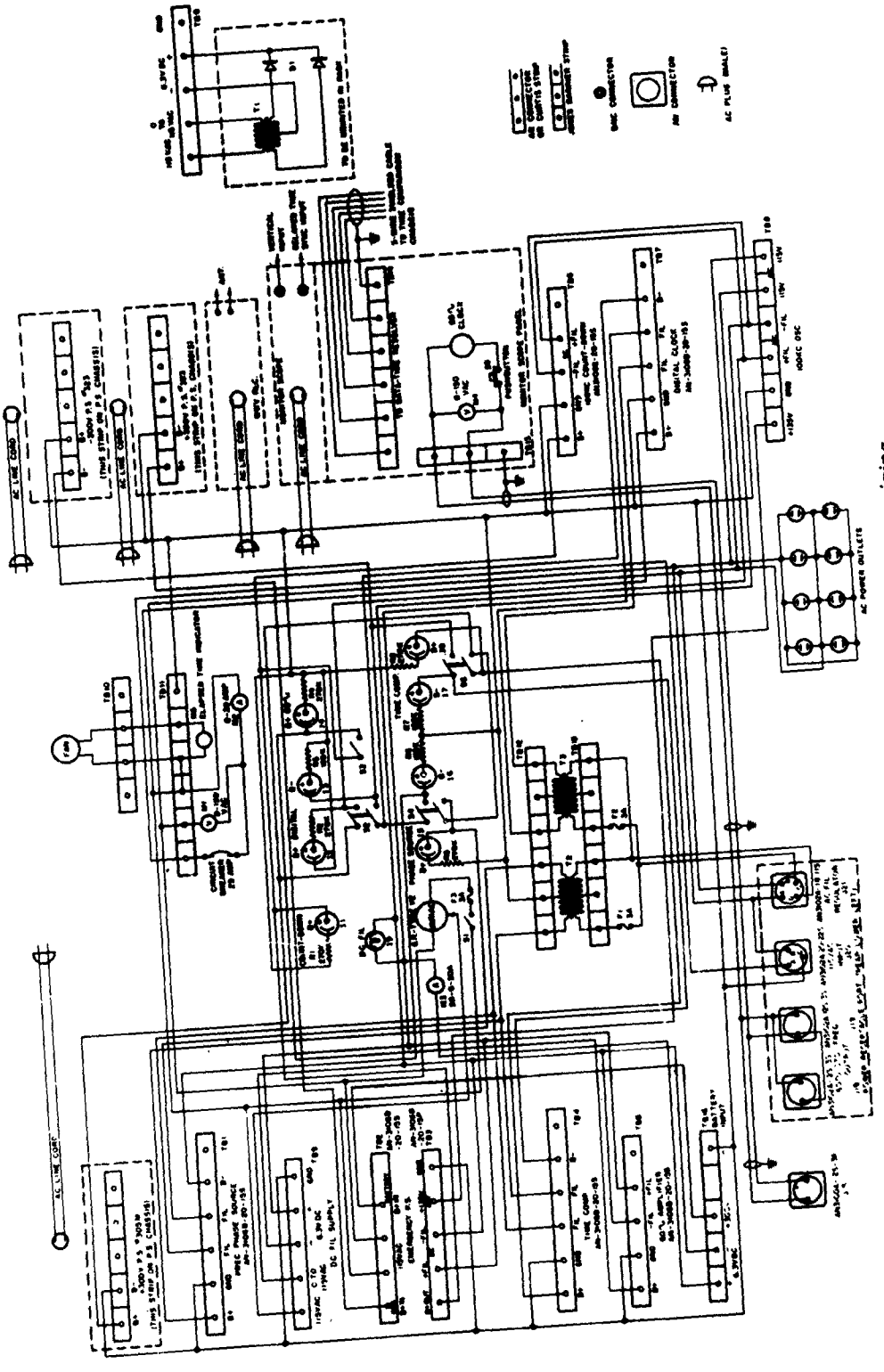

Fig. 17 - Time standard power wiring

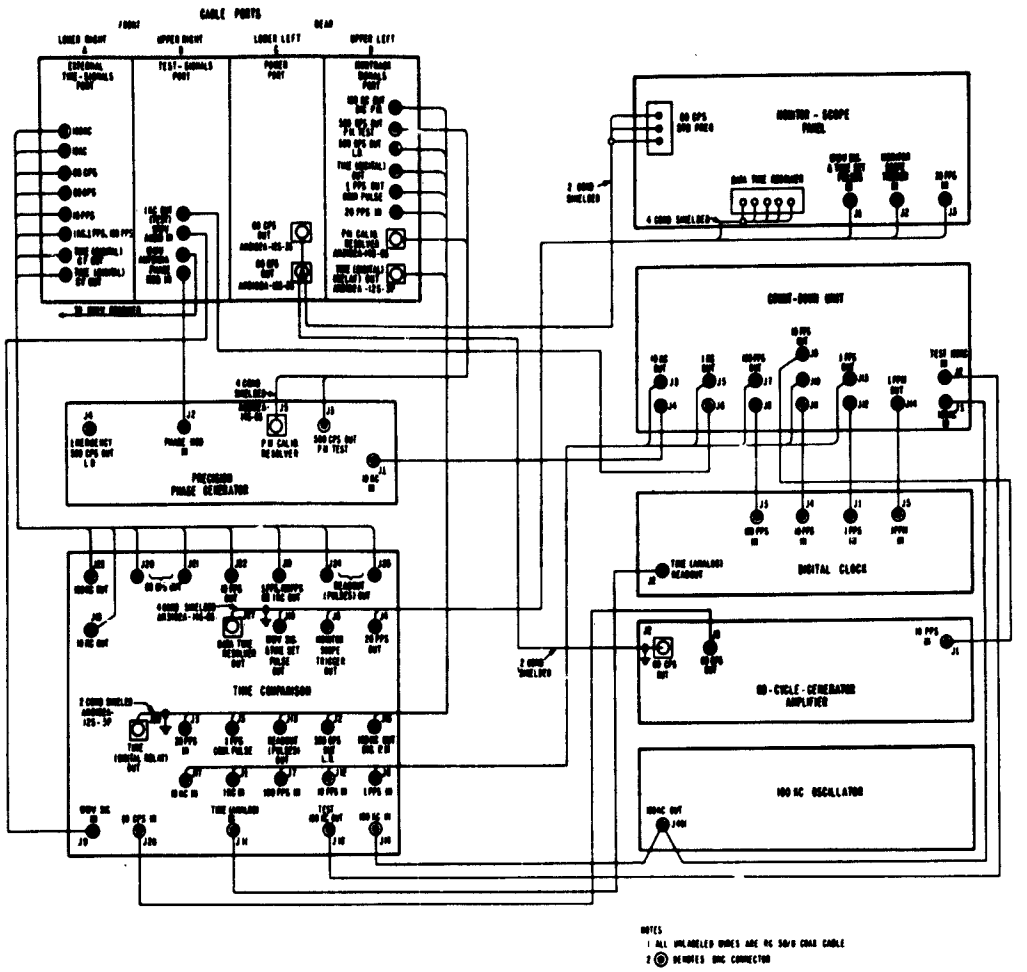


Fig. 18 - Time standard signal cable wiring

## 0-76A/U Oscillator

No adjustments other than small frequency corrections should be necessary for the 0-76A/U. The exact procedures to be followed depend upon the conditions encountered and the history of the oscillator. The output of the oscillator should be a 100-kc sine wave of approximately 6.3-volt rms amplitude.

## Count-Down Unit

Potentiometer R15 in the count-down unit should be adjusted for minimum amplitude variation at the cathode of V2B as the resolver phase shifter is turned. All outputs from the unit should have the proper frequency and amplitude. (See Appendix A for details.)

A brief procedure for adjusting the count-down unit to the correct time follows (this procedure assumes that the time-comparison circuits are in operation):

1. Reset the counters and release at the WWV time-tick marking the start of the minute or the return of the tone.

2. Synchronize the scope sweep to the sync output of the time-set pulse generator (positive pulse).

3. Observe the combined WWV time tick and the internally-generated marker pulse on the scope and adjust the resolver (phase-shifter at 10 kc) until the start of the time tick is coincident with the start of the sweep, and the internally-generated negative marker is coincident with the start of the second sine wave in the WWV time tick. Under conditions of long-distance reception some variation in the time of reception of the time tick will be noted. In general the earliest-arriving signal of a number of samples will be the most accurate.

## Digital Clock

The digital-clock chassis contains one adjustable potentiometer, R34. If, after connection of the proper input signals, the readout sequence counters fail to operate, the level of the reset bus should be checked and, if necessary, adjusted to ground potential when the serial-readout gate is open.

## Time Comparison Chassis

Time Comparison Circuit. – The only adjustment necessary in the time comparison circuit is the adjustment of the 1-millisecond phantastron to 1 millisecond (R115). This can be done using a 535 oscilloscope and the 10-kc and 1-kc outputs of the count-down unit.

500-cps Source. – No adjustments should be necessary to put the 500-cps source into operation. If excessive (over 5 percent) amplitude variation occurs in the output as the phase-shift resolver is turned, R30 should be adjusted to reduce this variation to a minimum.

Digital-Clock-Readout Circuit. – Once it has been determined that the serial-analog readout of the digital clock is correct, the adjustment of R190 and R136 can be made. R190, in connection with diode X9, determines the reference voltage level from which the phantastron V17 runs down. Therefore R190 should be set so that any level corresponding to the "zero" count in the digital clock will cause a rundown of about 50 milliseconds as measured at pin 6 of V17. Then adjust R136 so that any level corresponding to nine will cause a rundown of about 0.95 second. These two settings are somewhat interdependent, so that a compromise will have to be reached for the best settings of these controls. An auxiliary voltage source is furnished ("zero" level and "nine" level) for use in making the above adjustment. An alternate procedure is to adjust R190 to the center of the range giving one pulse out, adjust R136 to the center of the range giving 10 pulses out, and repeat once.

100-kc "Emergency" Oscillator. – The oscillator plate tank should be tuned for maximum output. C56 adjusts the frequency of the oscillator over a very limited range.

"Standard Time, Data Time" Coincidence Circuit. – No adjustments should be necessary for proper operation of the standard time, data time coincidence circuit.

### 60-cps Generator-Amplifier

Adjust R1 to obtain 115 volts rms across the "standard" clocks.

### Emergency-Power Transfer

Adjust R13 to give 135 volts dc to the 0-76A/U oscillator.

### Precision Phase Generator

The resolver phase shifter must be adjusted for proper phase difference (90°, R15) and equal amplitude (R12) on the two input windings. These adjustments can be made with sufficient accuracy by adjusting both for minimum amplitude variation out of the phase shifter as the resolver is turned. Adjust the amplitude first, then the phase, and repeat until the output-amplitude variation is reduced to a minimum.

## SUMMARY

The time standard described in this report is a basic part of the Minitrack satellite tracking system. With proper adjustment it is capable of maintaining a time reference at each station to ±1.0 millisecond.

All measurement frequencies with the exception of the local-oscillator frequencies used in the Minitrack system are derived from the basic time standard, and are phase-coherent. The practical effect of this is that the time of the start of any reading of the digital phase meters (Ref. 3) is known to within ±50 $\mu$sec with respect to the time standard. Time resolution from the actual phase records need be only to the nearest 0.05 second.

The time of day is read out in a serial code during the first 5 seconds of each 6-second interval. This code is available as relay contact closures (for the Sanborn Recorders; see Ref. 3) or as voltage pulses from a low-impedance source.

The serial time code and the various standard frequencies (100 kc, 10 kc, 1 kc, 100 cps, 10 cps, 1 cps) are available from transformer outputs suitable for feeding 50-ohm or 500-ohm lines.

Tests on the basic oscillator indicate a drift rate, due to crystal aging, of less than 1 part in $10^8$ per day (typical test result after several months' operation; 5 parts in $10^9$ per day). Tests with the time signals received at Washington from NBS Station WWVH indicate that a time setting within 1.0 millisecond, when working with a time signal from a distant station, is possible.

## ACKNOWLEDGMENTS

The authors wish to acknowledge the assistance of the members of the Tracking and Guidance Branch in the design and development of the Time Standard Equipment. They are, in addition, particularly indebted to Mr. Harris F. Hastings of the Radio Division, Radio Techniques Branch of the Laboratory.

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3. Schroeder, C.H., Looney, C.H., Jr., and Carpenter, H.E., Jr., "Project Vanguard Report No. 18, Minitrack Report No. 1, Phase Measurement," NRL Report 4995, 26 July 1957


* * *

## Appendix A

## MINITRACK TIME STANDARD DETAILED TEST SPECIFICATIONS

Unless otherwise specified, dc levels observed should be essentially the same as those given in the various tables, and in no case should they deviate by more than ±10 percent. Waveforms should be essentially as shown in the drawings. Levels with respect to ground and peak-to-peak swings should be essentially as shown, and in no case should they deviate by more than ±10 percent.

Power supplies used during tests shall be the same type as in the final equipment. B+ and B- voltages shall be set to within a volt of their specified value unless variation is specified as part of a test.

### 100-kc Oscillator (0-76A/U)

The 100-kc oscillator will be checked out in detail, and its drift rate determined, at NRL. The manufacturers instruction book gives the procedure for placing the unit in operation. After several hours of operation all outputs on its monitor meter should fall within the normal ranges listed in the instruction book. If the oscillator malfunctions it should be returned to NRL for repairs.

The oscillator obtains its B+ from the 135-volt regulator in the emergency-power transfer. This unit should be completely checked and adjusted before the oscillator is connected.

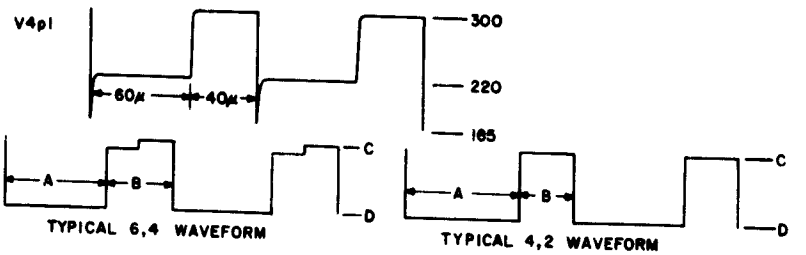
### Count-Down Unit

1. Connect the output of the 0-76A/U oscillator to J1 and the output of the "emergency oscillator" (time comparison connector J16) to J2. All counters should function properly with the signal from 0-76A/U or the emergency oscillator.

2. Waveforms observed at the various specified points are shown in the drawings of Fig. A1, which shows a typical 6,4 wave and a typical 4,2 wave from Hewlett-Packard AC-4A decade and modified decade counters. The points where these waves exist, the voltage amplitudes of the states with respect to ground, and the time scale, are also given.

3. With all signal inputs disconnected, the dc levels of the points listed in Table A1 should be checked.

4. Filament and B+ variations of ±10 percent should not affect operation of the count-down unit. No gain or loss of counts should be encountered over a 3-hour test period (1-1/2 hours with B+ and filaments 10 percent high, 1-1/2 hours with B+ and filaments 10 percent low).

| ITEM | POINT | WAVEFORM |
|---|---|---|
| 1 | V1p2 | SINE WAVE 12.5 V p-p, 33V CENTER PERIOD 10μs (100 KC) |
| 2 | V1p6 |   |
| 3 | K1p3 |   |
| 4 | V2p3 | SINE WAVE 60V p-p, 60V CENTER PERIOD 100μs (10KC) |
| 5 | V2p8 | SINE WAVE 30V p-p, 65V CENTER PERIOD 100μs (10KC) |
| 6 | V3p3 | SINE WAVE 28V p-p, 65V CENTER PERIOD 100μs (10KC) |
| 7 | V4p1 |   |

| | | A | B | C | D |
|---|---|---|---|---|---|
| 8 | K2p3 | 600μs | 400μs | 128V | 50V |
| 9 | V3p8 | 600μs | 400μs | 106V | 44V |
| 10 | K3p3 | 6ms | 4ms | 128V | 50V |
| 11 | V5p3 | 6ms | 4ms | 107V | 45V |
| 12 | K4p3 | 60ms | 40ms | 130V | 48V |
| 13 | V5p8 | 60ms | 40ms | 108V | 49V |
| 14 | K5p3 | 600ms | 400ms | 129V | 50V |
| 15 | V6p3 | 600ms | 400ms | 108V | 45V |
| 16 | K6p3 | 6SEC | 4SEC | 128V | 54V |
| 17 | K7p3 | 40SEC | 20SEC | 128V | 54V |
| 18 | V6p8 | 40SEC | 20SEC | 105V | 45V |

Fig. A1 - Count-down unit waveforms

Table A1
Count-Down Unit
Static DC Voltages

| Point | DC Volts | Point | DC Volts |
|---|---|---|---|
| V1p1 | 200 | V4p2 | 12 |
| V1p6 | 300 | V4p7 | 27 |
| V1p2 | 33 | V4p3, 8 | 26 |
| V1p7 | 27 | K2p3 | 52, 125, 130 |
| V1p3, 8 | 35 | V3p8 | 46, 105, 110 |
| K1p3 | 52, 112 | K3p3 | 52, 125, 130 |
| V2p3 | 69 | V5p3 | 48, 103, 110 |
| R11, R12, R13 | 66 | K4p3 | 56, 121, 130 |
| V2p8 | 71 | V5p8 | 48, 100, 109 |
| R17, R18, R19 | 67 | K5p3 | 52, 122, 130 |
| V3p3 | 65 | V6p3 | 46, 103, 110 |
| R21, R23, R24 | 62 | K6p3 | 54, 128, 136 |
| V4p1 | 300 | K7p3 | 53, 135 |
| V4p6 | 90 | V6p8 | 48, 110 |

60-cps Generator-Amplifier

Remove output tubes V2 and V3 and connect power to the chassis. Connect the 10-cps output of the count-down unit to the input connector J1. Adjust R1 to slightly over half scale and tune the first tank, L1,C1, to 60 cps (trim condenser C1: observation point, cathode of V1A). Repeat for the second tank, L2,C3. Replace V2 and V3 and adjust R1 for 115 volts rms across the load (two "standard" electric clocks). Sufficient range should be available on R1 to set this voltage 3 percent high. The dc voltage levels for the various points are listed in Table A2, and the ac swings in Table A3. The dc levels were taken with the input and the load connected and the unit in operation.

Table A2
60-CPS Generator-Amplifier
DC Voltages

| Tube No. | DC Volts | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 |
| V1 | 300 | 34 | 40 | H | H | 300 | 34 | 40 | H |
| V2 | 0 | 30 | H | H | 295 | 300 | 0 | -- | -- |
| V3 | 0 | 30 | H | H | 295 | 300 | 0 | -- | -- |

Table A3
60-CPS Generator-Amplifier
AC Swings

| Point | Peak-to-Peak Sine-Wave Amplitude (volts) |
|---|---|
| V1p3 | 12 |
| V1p8 | 25 |
| V2p1 | 60 |
| V3p1 | 60 |
| T2 output | 335 |

## Digital Clock

### General

Connect the 1-cps output of the count-down unit to J1, the 100-cps output to J3, the 10-cps output to J4, and the 1-cpm output to J5. The circuits on this chassis must be checked for operation in the following order:

1. Input circuits V1, counter K1, and one-shot multivibrator V2.

2. Time-indicating counters K2, K3, K4, K5, K6 and the "24-hour" reset circuits V11, V12, and V13A.

3. Time readout circuits, sequence counters V7, V8, V9 and reset circuits V13B and V14.

The normal input to the digital clock is the 1-cps output from the count-down unit. Waveforms in Fig. A2 are shown for the normal signal-input conditions unless otherwise specified.

Extra counts may be introduced into the system by placing the vtvm or scope probe on certain critical points in the circuit. These sensitive points are: V1p6; V2p2, 6, 7; V3p6; V11p2, 6, 7; V13p2; K2p3, 5; K3p3, 5; K4p3, 5; K5p3, 5, 9, 10; K6p3, 5, 9, 10. Unless otherwise specified, the dc voltages are taken with the input to the digital clock removed.

### Detailed Specifications

1. Check the dc levels for items 1 through 11 (V1, V2, and K1) in Table A4.

2. Observe the waveforms for items 1 through 7 in Fig. A2.

3. Check the operation of the time-indicating counters for proper counting and reset sequence as indicated in Table A5. (Switch S3 can be set to 10-per-second or 100-per-second positions to observe action of lower speed counters.)

4. Check the dc voltages for items 12 through 23 in Table A5 (counters and reset circuits V11, V12, and V13A) with the input to J1 removed and switch S2 in the normal position.

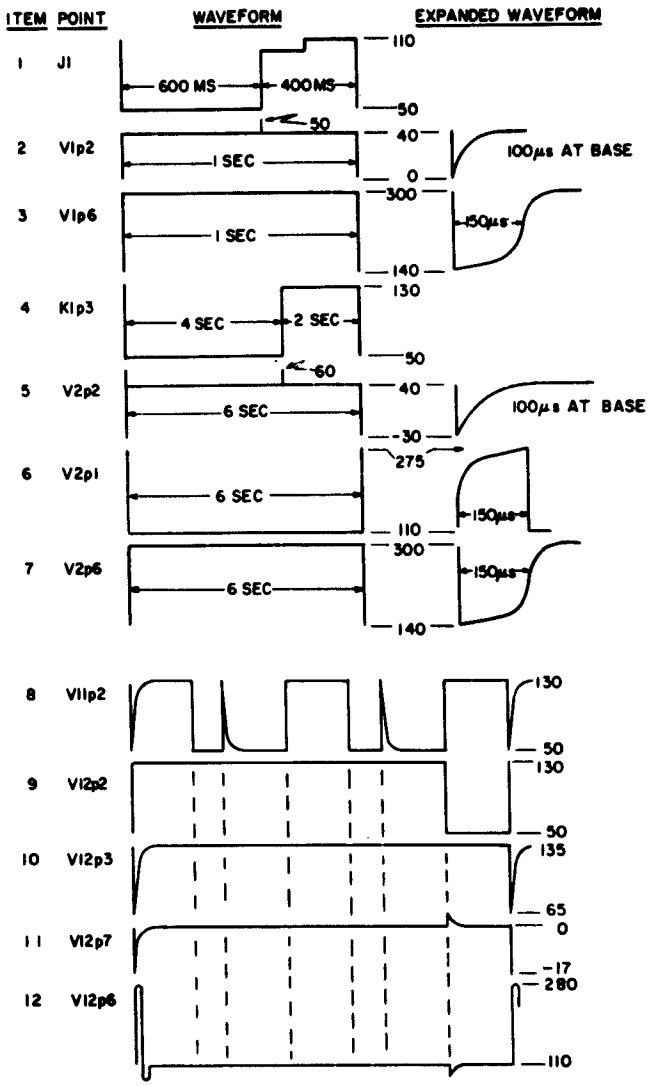



Fig. A2 - Digital clock waveforms

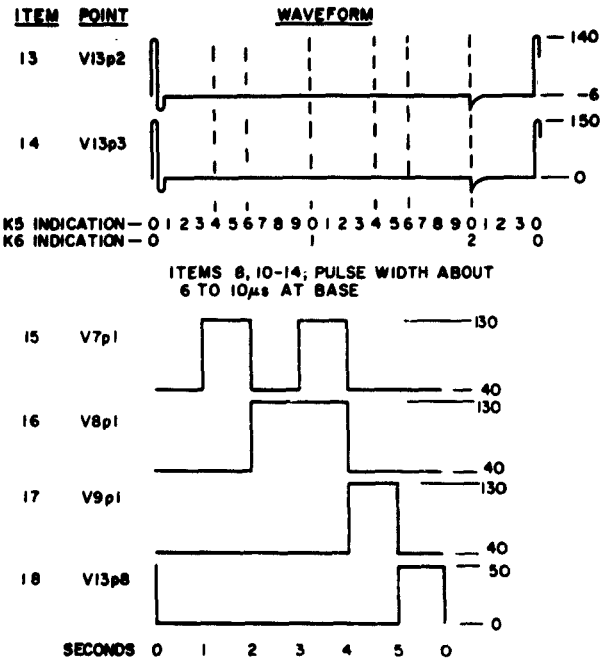



Fig. A2 (Continued) - Digital clock waveforms

**Table A4**
**Counter Operation**

| Counter | Indicates | Resets at (Time) | Indicator Lights |
|---|---|---|---|
| K1, ÷ 6 | Seconds | End of 6th Second | 0 through 5 |
| K2, ÷ 10 | 0.1 Minute | End of Minute | 0 through 9 |
| K3, ÷ 10 | Minutes | End of 10th Minute | 0 through 9 |
| K4, ÷ 6 | 10's of Minutes | End of Hour | 0 through 5 |
| | Hours | End of 10 Hours | 0 through 9 |
| K5, ÷ 10 | Hours | End of 20 Hours | 0 through 9 |
| | Hours | End of 24 Hours | 0 through 3 |
| K6, ÷ 10 | 10's of Hours | End of 24 Hours | 0 through 2 |

Table A5
Digital Clock Static DC Voltage Readings*

| Item | Point | DC Volts | Item | Point | DC Volts |
|---|---|---|---|---|---|
| 1 | V1p2 | 41 | 24 | V7p2 | 11, 22, 28 |
| 2 | V1p7 | 0.5 | 25 | V7p7 | 24, 11, 10 |
| 3 | V1p1 | 90 | 26 | V7p1 | 125, 40, 35 |
| 4 | V1p6 | 300 | 27 | V7p6 | 40, 125, 125 |
| 5 | V1p3, 8 | 41 | 28 | V7p3, 8 | 24, 23, 28 |
| 6 | K1p3 | 52, 135 | 29 | V8p2 | 11, 24, 28 |
| 7 | V2p2 | 40 | 30 | V8p7 | 24, 11, 10 |
| 8 | V2p7 | 0 | 31 | V8p1 | 125, 40, 35 |
| 9 | V2p1 | 110 | 32 | V8p6 | 40, 125, 125 |
| 10 | V2p6 | 300 | 33 | V8p3, 8 | 24, 23, 28 |
| 11 | K2p3 | 52, 125, 135 | 34 | V9p2 | 11, 23, 28 |
| 12 | K3p3 | 52, 125, 135 | 35 | V9p7 | 24, 11, 10 |
| 13 | K4p3 | 50, 135 | 36 | V9p1 | 125, 40, 35 |
| 14 | K5p3 | 50, 135 | 37 | V9p6 | 40, 125, 125 |
| 15 | V11p2 | 46, 130 | 38 | V9p3, 8 | 24, 23, 28 |
| 16 | V11p3, 8 | 130 | 39 | V3p2 | 14, 29 |
| 17 | V12p2 | 50, 142 | 40 | V3p7 | 27, 13 |
| 18 | V12p3 | 130, 145 | 41 | V3p1 | 130, 48 |
| 19 | V12p7 | 0 | 42 | V3p6 | 50, 140 |
| 20 | V12p8 | 0.8 | 43 | V3p3, 8 | 26, 28 |
| 21 | V12p6 | 110 | 44 | V10p3, 8 | 130 |
| 22 | V13p2 | -5 | | | |
| 23 | V13p3 | 3.5 | | | |

*Voltages positive unless otherwise indicated.

5. Observe the waveforms for items 8 through 14 in Fig. A2. The following arrangement is suggested for this observation:

a. 1-kc input to J1.

b. Synchronize scope to V2p6.

c. Connect V2p6 to K5p5 to obtain 1-kc input to K5.

6. Adjust the reset bus (R34) of sequence counters V7, V8, and V9 to the center of its operating range. (If the counters are not operating properly, assume zero volts with respect to ground in the counting condition as the proper setting.) The reset-bus operating range should be from approximately -3 to +5 volts dc, and in no case should the positive

or negative limit of this operating range be less than 2 volts with respect to ground nor the total range less than 6 volts. Items 15 through 17 in Fig. A2 indicate proper operation of the sequence counters. DC voltages for the various states of the sequence counters are given in Table A5, items 24 through 38.

7. The dc voltages for the time-readout-gate multivibrator, V3, and the reset gate, V10, are given in Table A5, items 39 through 44. Since V3p6 controls the sequence-counter reset bus, the plate waveform is the same as shown in Fig. A2, item 18, except for level and amplitude. The base level of the waveform on V3p6 is approximately +50 volts and the amplitude of the swing 120 volts. The waveform at the cathode of V10 is simply a fall (at count "five") which is differentiated and used to close the gate, V3.

8. With a 1-kc input to J1 and with the scope properly synchronized, it is possible to view all analog time-readout levels simultaneously. The count adjustment of the readout-bus levels is given in Table A6.

Table A6
Serial Analog Readout Levels* from J2

| Counter No. K- | | 6 | 5 | 4 | 3 | 2 | |
|---|---|---|---|---|---|---|---|
| Time (Seconds) | 0 | 1 | 2 | 3 | 4 | 5 | 0 |
| Typical | 138 | | -0- | -0- | -0- | -0- | --- |
| Readout | 128.7 | -0- | -1- | -1- | -1- | -1- | |
| Levels | 119.3 | -1- | -2- | -2- | -2- | -2- | |
| Volts, DC | 110 | -2- | -3- | -3- | -3- | -3- | |
| | 100.7 | | -4- | -4- | -4- | -4- | |
| | 91.3 | | -5- | -5- | -5- | -5- | |
| | 82 | | -6- | | -6- | -6- | |
| | 72.7 | | -7- | | -7- | -7- | |
| | 63.3 | | -8- | | -8- | -8- | |
| | 54 | | -9- | | -9- | -9- | |

*"-3-" etc., indicates state of counter.

Some variation of staircase level is to be expected from the normal Hewlett-Packard AC-4A counters. The "zero" and "nine" levels in Table A6 will be defined as the average of the "zero" or "nine" levels of counters K2, K3, and K5 as measured on the readout bus, provided their total spread at the "zero" or "nine" level is no greater than 4 volts. Eight voltage levels (nine intervals) should be defined between these two levels and no single level should be more than +2 volts from the defined level. The "zero" level for the sixth second can be adjusted by changing R21. Note that the "zero" level for K6 is adjusted to be the same as the "one" level for the other counters.

9. The time-indicating counters K1 through K6 should continue to operate for B+ supply variations of ±10 percent. The sequence counters V7, V8, and V9 and the associated reset circuits should operate over a B+ range of ±5 percent. The analog-readout levels are not expected to retain the correct value with B+ variations.

## Time Comparison Chassis

### General

The time comparison chassis consists of a number of different circuits performing various functions in the time standard; separate test specifications are given for each of these circuits. The dc voltages taken with zero input-signal level are listed in Table A7 and the waveforms are shown in Fig. A3.

Table A7
Time Comparison Chassis
Tube Pin Voltages

| Tube No. | DC Volts | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 |
| V1 | 92 | 42 | 41.5 | H | H | 300 | 0 | 41.5 | H |
| V2 | 49 | 30 | 30 | H | H | 50 | 30 | 30 | H |
| V3 | 300 | 39 | 42 | H | H | 208 | 10.5 | 13.2 | H |
| V4 | 300 | -1.9 | 1.5 | H | H | 300 | 0 | 4.2 | H |
| V5 | 112 | 22.3 | 22.8 | H | H | 300 | 0 | 22.8 | H |
| V6 | 300 | -60 | -30 | H | H | 52 | 30 | 30 | H |
| V7 | 112 | 38 | 39 | H | H | 300 | 0 | 39 | H |
| V14 | 20.5 | 20 | H | H | 110 | 56 | 11 | --- | --- |
| V15 | 300 | 56 | 60 | H | H | 300 | 55 | 60 | H |
| V16 | 300 | 140 | 143 | H | H | 176 | 0 | 2.7 | H |
| V17 | 0.41 | 0 | H | H | 135 | 44.5 | -40 | --- | --- |
| V18 | 300 | -9.1 | 0.28 | H | H | 300 | 0 | 6.5 | H |
| V19 | 278 | 15.8 | 34 | H | H | 108 | 34 | 34 | H |
| V20 | -0.54 | 0 | H | H | 285 | 35 | 0 | --- | --- |
| V21 | 300 | 92.5 | 95 | H | H | 300 | 92.5 | 95 | H |
| V22 | 300 | 3.9 | 7.8 | H | H | 300 | 3.9 | 7.8 | H |
| V23 | 300 | 4.3 | 8.8 | H | H | 300 | 4.2 | 8.6 | H |
| V24 | 300 | 4.0 | 8.1 | H | H | 300 | 3.8 | 7.9 | H |
| V25 | 300 | 4.2 | 8.2 | H | H | 300 | 4.0 | 7.9 | H |

### Digital-Clock-Readout Circuit

Connect the time readout from the digital clock or the special test unit, mentioned below, to J11, the 1-cps output of the count-down unit to J6 and the 10-cps output to J12. The circuit must first be adjusted to pass the proper number of 10-cps pulses for the various levels. A small test unit, consisting of two cathode followers with adjustable levels, has been developed to facilitate this adjustment. Power for the test unit is supplied by J29. Adjust the test unit so that one cathode stands by at the "zero" level of the

digital-clock-readout bus and the other at the "nine" level. Switch to the "zero" level and adjust R190 so that one pulse per second is passed by the circuit* (center of the range for passing one pulse). Switch to the "nine" level and adjust the phantastron rundown time (R136) to the center of the range for passing 10 pulses per second.* Since there is a slight amount of interaction, repeat the adjustment one. The waveforms are shown in Fig. A3, items 1 through 9.

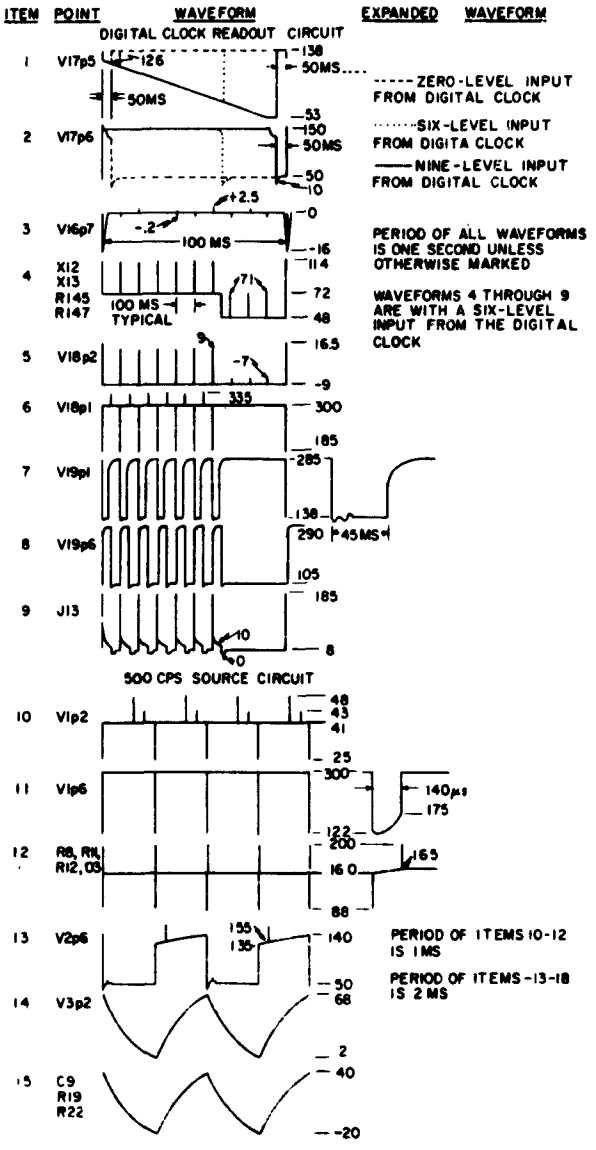



Fig. A3 - Time comparison chassis waveforms

*Phantastron run-down times of 50 milliseconds and 950 milliseconds for the "zero" and "nine" levels respectively

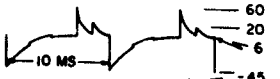
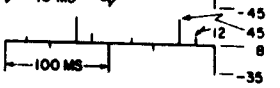
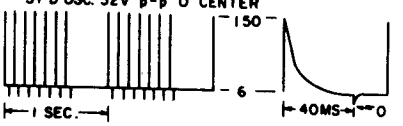
| ITEM | POINT | WAVEFORM |
|---|---|---|
| | | CATHODE FOLLOWER CIRCUITS |
| 34 | V22p8 | SINE WAVE, 10 KC<br>20V p-p, 8V CENTER |
| 35 | V22p3 |  |
| 36 | V24p8 |  |
| 37 OR 38 | V23p8 OR V23p3 | SINE WAVE, 60 CPS<br>55V, p-p, 6.5V CENTER |
| 39 | V24p3 | SINE WAVE, 100KC EMER'CY OSC. 48V p-p, 0V<br>ST'D OSC. 52V p-p 0 CENTER |
| 40 OR 41 | V25p3 OR V25p8 |  |
| | | 100 KC EMERGENCY OSCILLATOR CIRCUIT<br>USED AS OSCILLATOR |
| 42 | S4,C58 | SINE WAVE, 100KC<br>60V p-p, 0V CENTER |
| 43 | XTAL PIN 3 | SINE WAVE, 100KC<br>60V p-p, 0V CENTER |
| 44 | V20p5 | SINE WAVE, 100KC<br>260V p-p, 290V CENTER |
| 45 OR 46 | J15 OR J16 | SINE WAVE, 100KC<br>125V p-p, 0V CENTER |
| 47 | J23 | SINE WAVE, 100KC<br>6V p-p, 0V CENTER |
| | | USED AS AMPLIFIER |
| 48 | S4,C58 | SINE WAVE, 100KC<br>13V p-p, 0V CENTER |
| 49 | V20p5 | SINE WAVE, 100KC<br>300V p-p, 290V CENTER |
| 50 OR 51 | J15 OR J16 | SINE WAVE, 100KC<br>130V p-p, 0V CENTER |
| 52 | J25 | SINE WAVE, 100KC<br>7V p-p, 0V CENTER |

Fig. A3 (Continued) - Time comparison chassis waveforms

The digital-clock-readout circuit should continue to operate with a ±10 percent variation of B+ or B-; however, the correct number of pulses may not be produced for a given level from the digital clock under these conditions.

100-kc "Emergency" Oscillator

In adjusting the frequency of this oscillator to match that of the standard oscillator (0-76A/U) the scope probe should be placed on the cathode on one of the output cathode followers (V21) and not on the oscillator circuits. The amplitude of the output sine wave should be approximately 120 volts peak-to-peak, and C56 and C61 should be near the center of their adjustment ranges. No waveform drawings are given for this circuit. With switch S4 in the "amplifier" position and the input from the 0-76A/U connected, the outputs from V21 should be essentially the same as when the circuit is operating as an oscillator.

500-cps Source

Connect the 1-kc output from the count-down unit to J1. Adjust R30 for minimum variation in output amplitude as the resolver phase-shifter is turned. The output should be a sine wave approximately 40-volt peak-to-peak amplitude. Waveforms at the more important points in the circuit are given in Fig. A3, items 10 through 18. This circuit should operate satisfactorily with a B+ variation of ±10 percent.

"Standard Time, Data Time" Coincidence Circuit

Connect the special test unit mentioned above to J11, the 1-cps output from the count-down unit to J6, the 10-cps output to J12, and a lead from J13 to J3. Connect a 68K resistor to J5 and in series with an NE2 neon lamp to ground.

With the test unit set to the zero level position, the neon lamp should flash for approximately 50 milliseconds once per second. Reducing the signal on either J3 or J6 to zero should cause the lamp to stop flashing. No partial-coincidence pulse should come within 10 volts of the voltage necessary to trigger the output multivibrator. The waveforms are shown in Fig. A3, items 19 through 24. This circuit should operate satisfactorily with a B+ or B- variation of ±10 percent.

Time-Set-Pulse Generator

Connect the 1-cps output from the count-down unit to J6. The phantastron, V14, should have a fixed delay of 1 millisecond, and can be adjusted to this by means of R115. Waveforms of the more important points in the circuit are shown in Fig. A3, items 25 through 32. The circuit should continue to operate for a ±5 percent change in B+ or B-; however, the delay set in by the phantastron may change somewhat.

Cathode-Follower Output Circuits

Connect the proper signal to the cathode-follower input jack and a 500-ohm or 50-ohm resistance to the output jack, as indicated on the schematic. The waveforms at the cathodes are given in Fig. A3, items 33 through 40. These circuits should operate satisfactorily with a B+ variation of ±10 percent.

## Precision Phase Generator

1. Connect a Reeves R-150 resolver to J5 and set the toggle switch to the "unmodulated" position. Table A8 shows the dc voltage levels with zero signal input on J1 and J2.

2. Connect the 10-kc sine wave from the count-down unit to J1. Figure A4 shows the waveforms, and Table A9 lists the ac swings.

**Table A8**
**Precision Phase Generator**
**Tube Pin Voltages**

| Tube No. | DC Volts | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 |
| V1 | 300 | 41 | 45 | H | H | 253 | 45 | 47 | H |
| V2 | 300 | 37 | 41 | H | H | 300 | 47 | 50 | H |
| V3 | 300 | 50 | 52 | H | H | 300 | 48 | 50 | H |
| V4 | 300 | 35 | 39 | H | H | --- | --- | --- | H |
| V5 | 90 | 35 | 28 | H | H | 300 | 12 | 28 | H |
| V6 | 48* | 30* | 29 | H | H | 145* | 13* | 29 | H |
| V7 | 300 | 39 | 44 | H | H | 215 | 9.4 | 12 | H |
| V8 | 300 | 10 | 14 | H | H | 300 | 10 | 14 | H |
| V9 | 300 | 55 | 60 | H | H | 300 | 34 | 39 | H |
| V10 | 300 | 0 | 4.1 | H | H | --- | --- | --- | H |
| V11 | 300 | 68 | 71 | H | H | 300 | 71 | 76 | H |
| V12 | 18 | 18 | H | H | 72 | 56 | 11 | --- | --- |

*Pins 1 and 2 may have their voltages interchanged with pins 6 and 7 of the same tube, depending on the state of the tube.

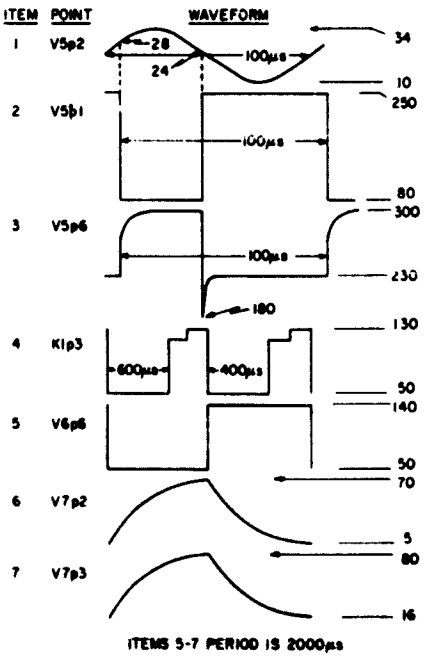



**Fig. A4 - Precision phase generator waveforms**

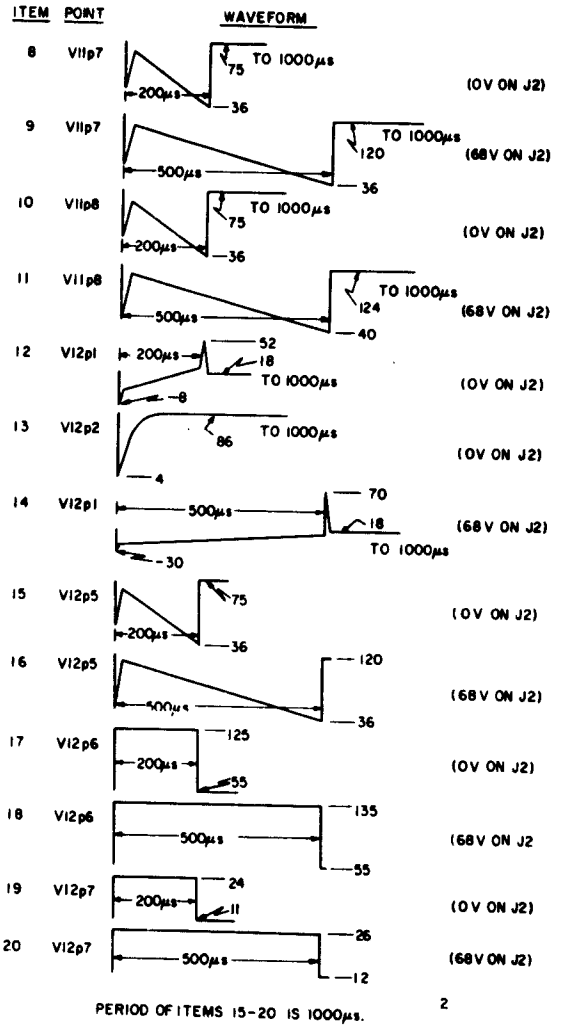



**Fig. A4 (Continued) - Precision phase generator waveforms**

Table A9
Precision Phase Generator
AC Swings

| Item | Point | P-P Volts | Center Volts | Period | Phase |
|---|---|---|---|---|---|
| 1 | J1 | 32 | 64 | 100 | 0 |
| 2 | V1p2 | 30 | 42 | 100 | 0 |
| 3 | V1p3 | 28 | 46 | 100 | 0 |
| 4 | V1p7 | 30 | 46 | 100 | 0 |
| 5 | V1p8 | 32 | 46 | 100 | 0 |
| 6 | V1p6 | 32 | 262 | 100 | 180 |
| 7 | V2p2 | 26 | 28 | 100 | 180 |
| 8 | V2p3 | 24 | 43 | 100 | 180 |
| 9 | V2p7 | 26 | 47 | 100 | 0 |
| 10 | V2p8 | 25 | 52 | 100 | 0 |
| 11 | V3p8 | 26 | 53 | 100 | 0 |
| 12 | V3p3 | 20 | 53 | 100 | 90 |
| 13 | J5pF | 30 | 0 | 100 | Variable |
| 14 | V4p3 | 34 | 40 | 100 | Variable |
| 15 | V5p2 | 24 | 22 | 100 | Variable |
| 16 | V7p7 | 9 | 7.5 | 2000 | Variable |
| 17 | V7p6 | 45 | 212 | 2000 | Variable |
| 18 | V9p7 | 48 | 38 | 2000 | Variable |
| 19 | V9p8 | 46 | 59 | 2000 | Variable |
| 20 | V8p2, 7 | 32 | 8 | 2000 | Variable |
| 21 | V8p3, 8 | 28 | 16 | 2000 | Variable |
| 22 | V9p2 | 27* | 22 | 2000 | Variable |
| 23 | V9p3 | 26* | 40 | 2000 | Variable |

*R56 set for maximum signal

3. Adjust R15 to give a 90° phase difference between the signals on the cathodes of V3A and V3B, and adjust R12 so that these signals are of equal amplitude.*

4. The output phase should shift smoothly and continuously as the resolver is turned, the phase of the 500-cps output shifting 18° for each revolution of the resolver.

5. Connect a variable dc voltage source to J2 and throw the toggle switch to the "modulated" position. The relative phase of the 500-cps output should change in a nearly linear manner at least 20 degrees as the dc voltage level on J2 is varied from -15 to +15 volts (Fig. A5).

*Final adjustments must be made on the basis of minimum amplitude variation of output as the resolver is turned. (See the discussion of the 500-cps source.)

## Appendix B

## LIST OF AC-4A DECADE COUNTER MODIFICATIONS

### Conversion to Scale of Six for Tens-of-Seconds Counter in Count-Down Unit

1. Remove V4.
2. Remove R43, 44, 46, and 47 (all 220K, 1/2 watt).
3. Remove I7, 8, 9, and 10 (Ne-2 bulbs).
4. Remove R23 (220K, 1/2 watt).
5. Remove R38 (1.5 Meg., 1/2 watt).
6. Remove C13 (47 $\mu\mu f$).
7. Remove R51 (180K, 1/2 watt) and C17 (75 $\mu\mu f$).
8. Add a 220K 1/2-watt resistor from V3p1 to the bus tied to the common connection between I1 and I2.
9. Remove the connection of R52 (150K 1/2 watt) from V3p1 and connect to V3p6.
10. Remove the connection of C18 (39 $\mu\mu f$) from V2p7 and connect to V2p2.
11. Make a connection from the bus tied to the common connection between I5 and I6 to the bus originally tied to the common connection between I9 and I10.
12. Disconnect the output lead from V4p1 and connect to V3p1.

### Conversion to Scale of 6 for Seconds and Tens-of-Minutes Counter in Digital Clock

This procedure is the same as that described above for the count-down unit.

### Conversion to Hours and Tens-of-Hours Counters for Digital Clock

1. Remove the octal plug and replace it with an 11-pin plug, making sure that mechanical alignment is correct.
2. Reconnect pins 1 through 8 as they were in the octal plug.
3. Connect an insulated wire (No. 20) from pin V3p6 to pin 9 of the 11-pin plug.
4. Connect an insulated wire (No. 20) from V2p6 to pin 10 of the 11-pin plug.

FR 4748 - ADC 343044
4767 - ADO 341439
4728 - ADO 340793
4717 - not in DTIC
4800 - ADC 342755
4815 - ADO 342991
4860 - ADO 342505
4880 - ADO 343187
4890 - ADO 343093
4900 - ADO 342883
4910 - ADO 343031
4930 - ADO 342912
4950 - ADC 342643
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